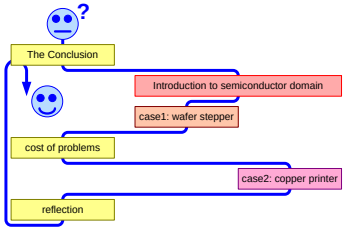
Save Money by Investing In Models; Failing Early is More affordable Than Failing Late

by *Gerrit Muller* University of South-Eastern Norway-NISE
e-mail: gaudisite@gmail.com
www.gaudisite.nl

Abstract

Many stakeholders in systems development are unaware of the unknowns. Making and using virtual and physical models helps to validate assumptions, to calibrate the understanding, and to identify uncertainties and unknowns. A major risk is that some stakeholders think that they can afford to skip the laborous phase of trial, error, trouble shoot, and validation. It is an old wisdom that it is less costly to fail early than to fail late. We will use two cases from the semiconductor industry for illustration.

July 3, 2023
status: preliminary draft
version: 0.1



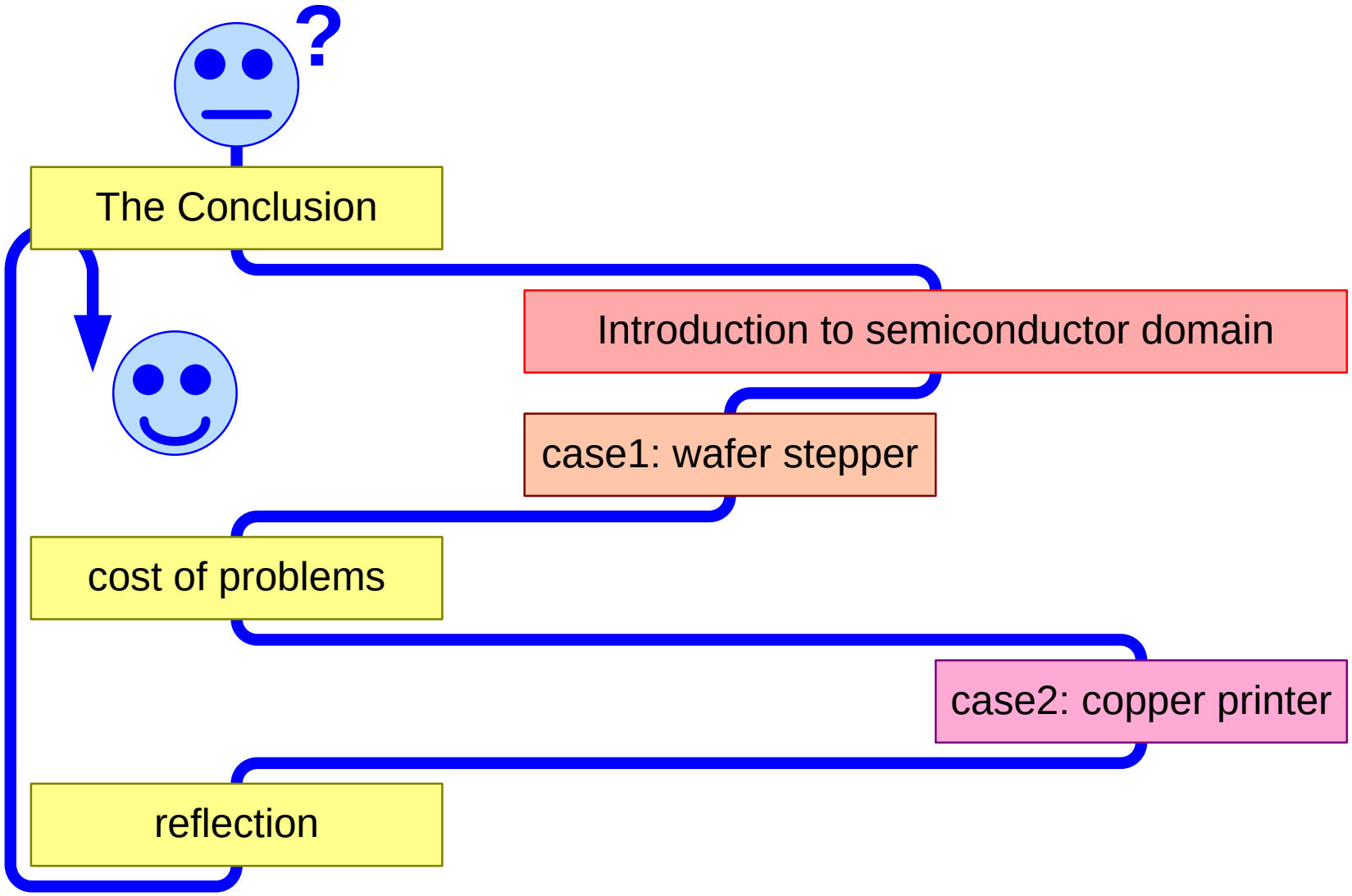
The Final Conclusion

Early ***investments*** in

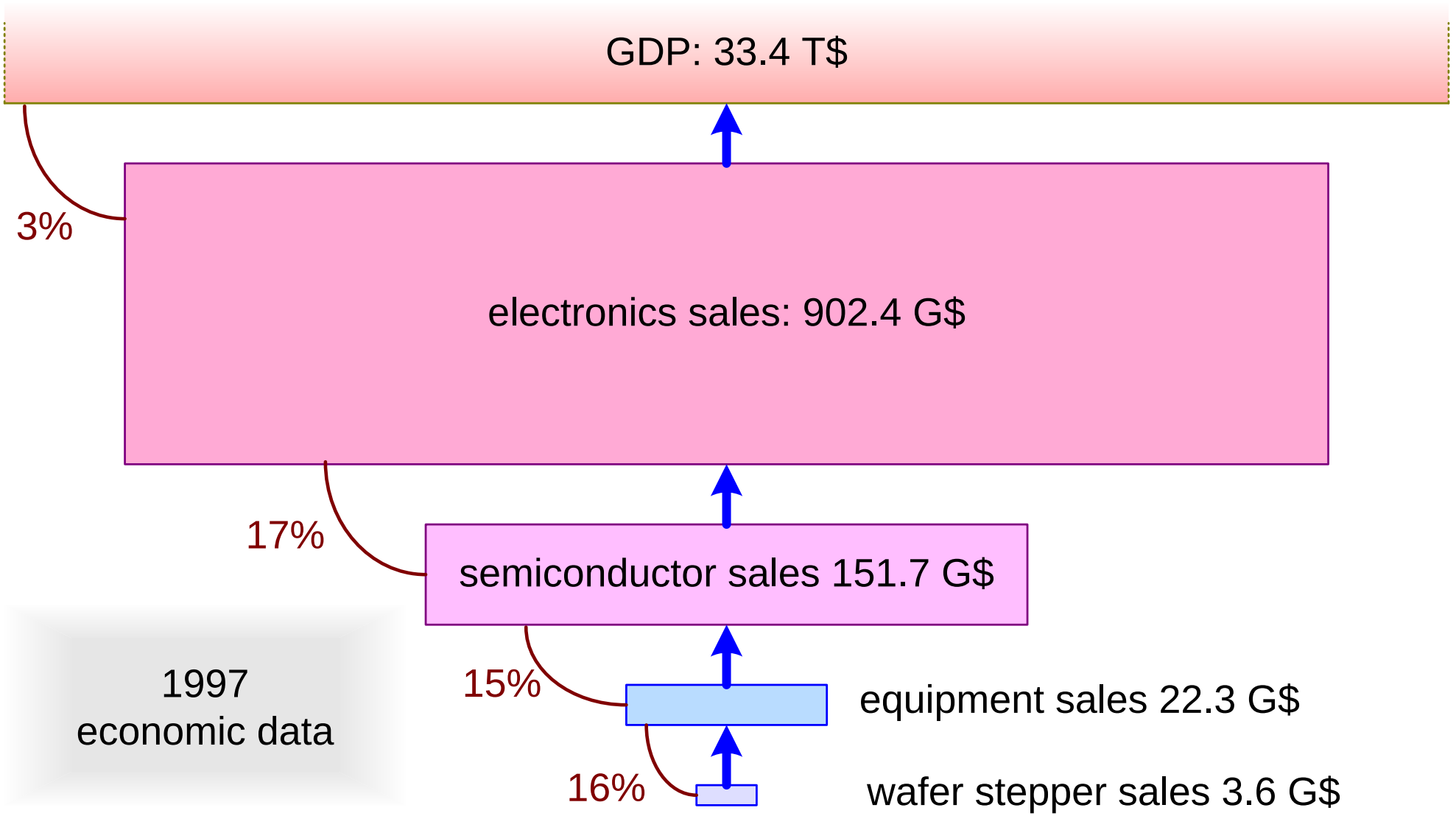
test rigs, prototypes, virtual models, and simulations

save a lot of money

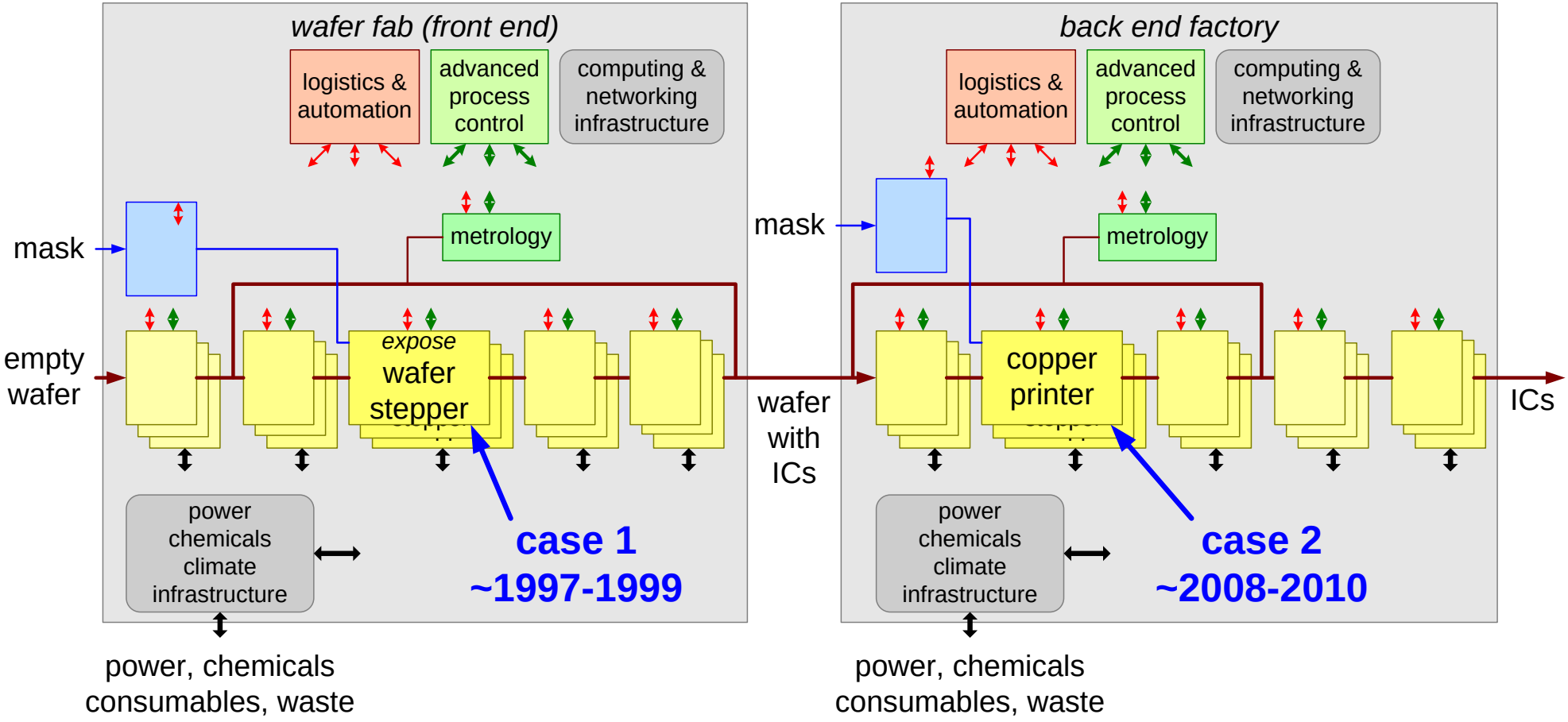
Figure Of Contents™



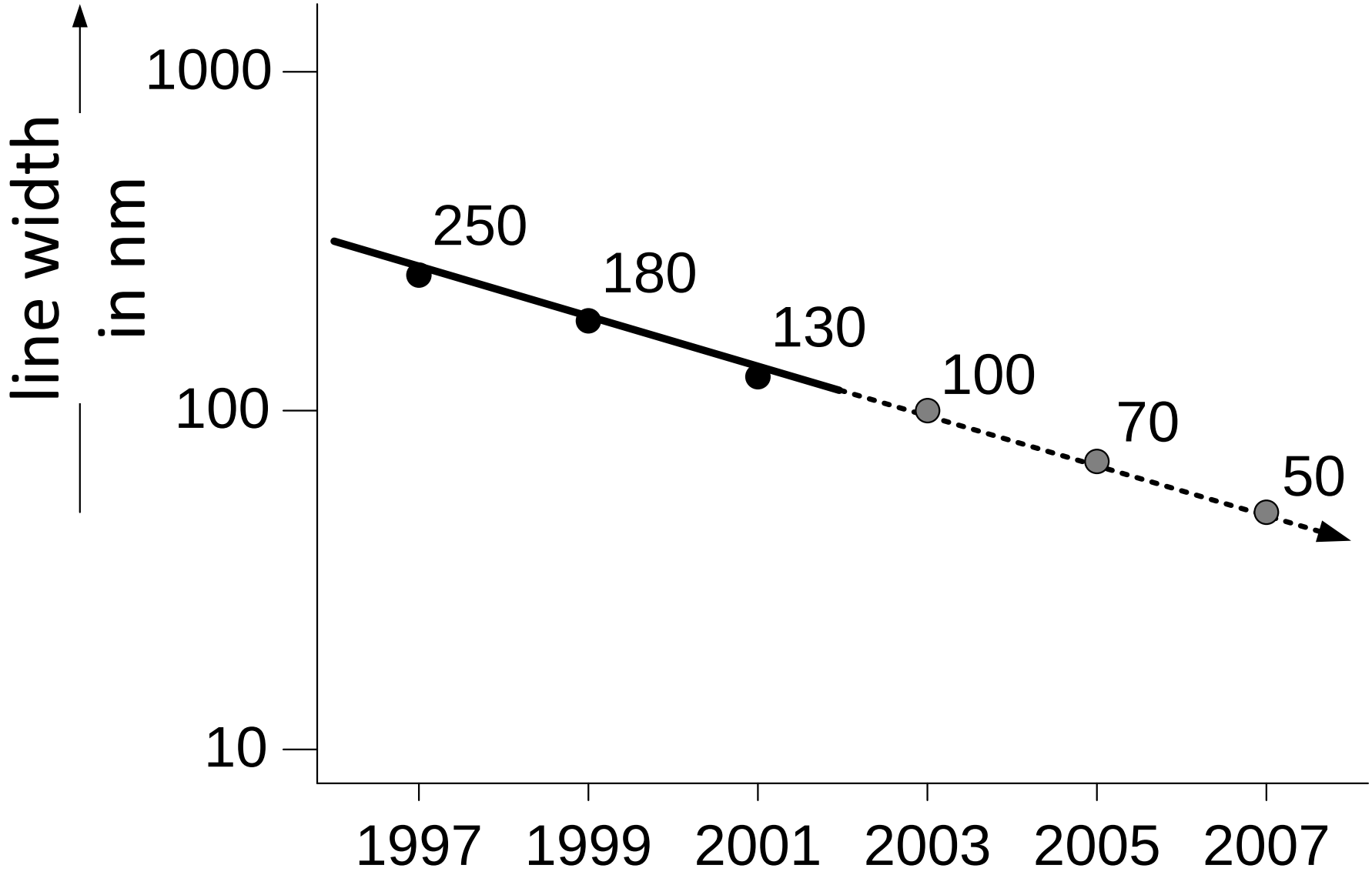
Semiconductor Economics

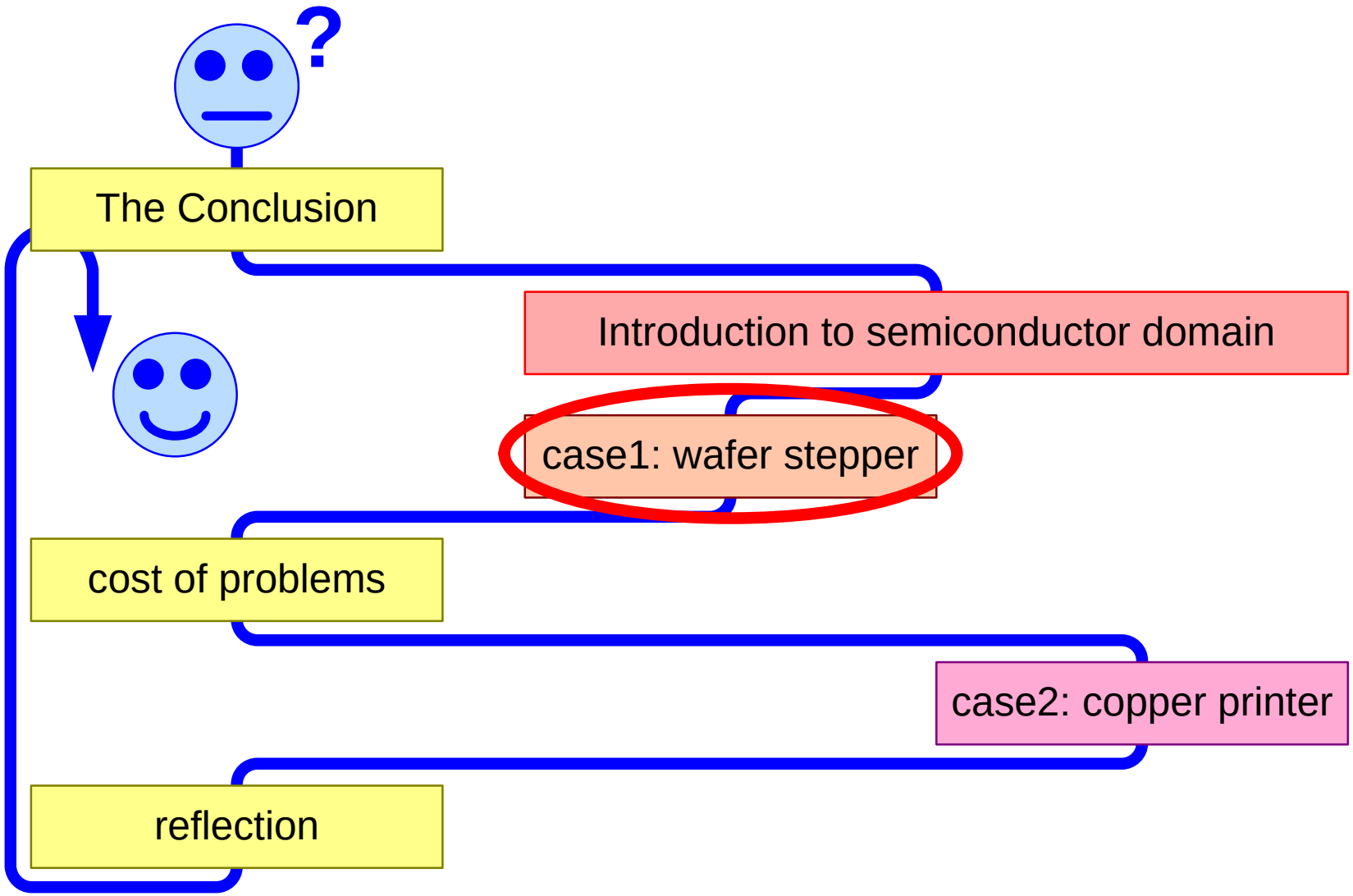


Semiconductor IC manufacturing



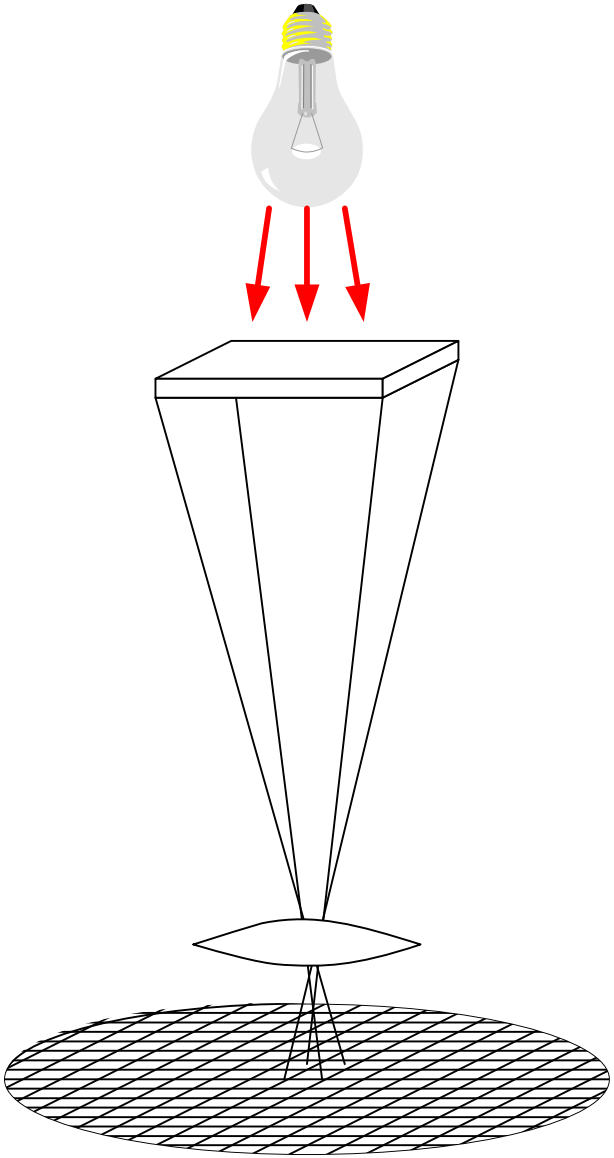
Moore's law


line width
in nm
1000
100
10
250
180
130
100
70
50
1997
1999
2001
2003
2005
2007


The Conclusion
Introduction to semiconductor domain
case1: wafer stepper
cost of problems
case2: copper printer
reflection

Twinscan AT1100

What is a waferstepper



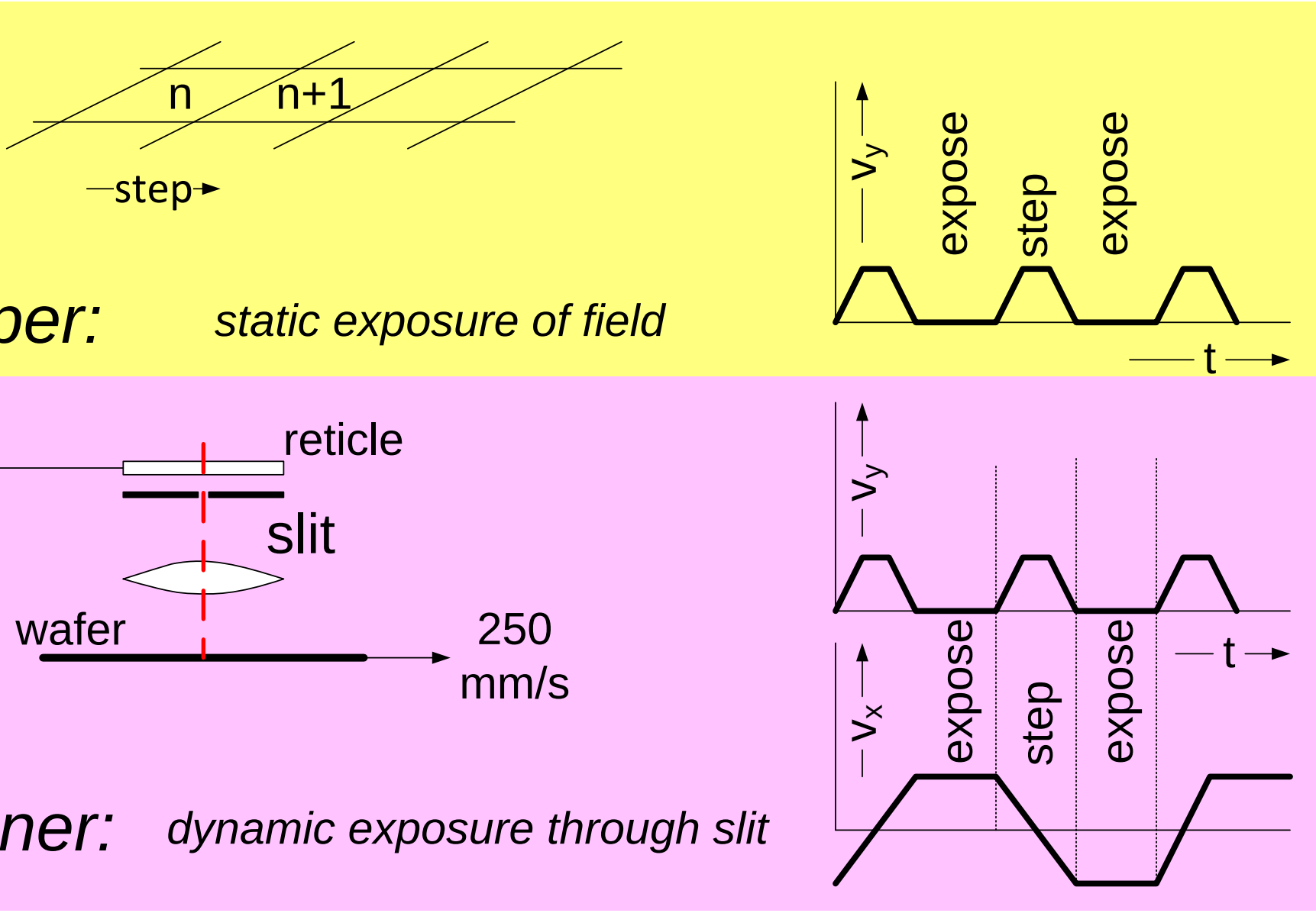
source

reticle

lens

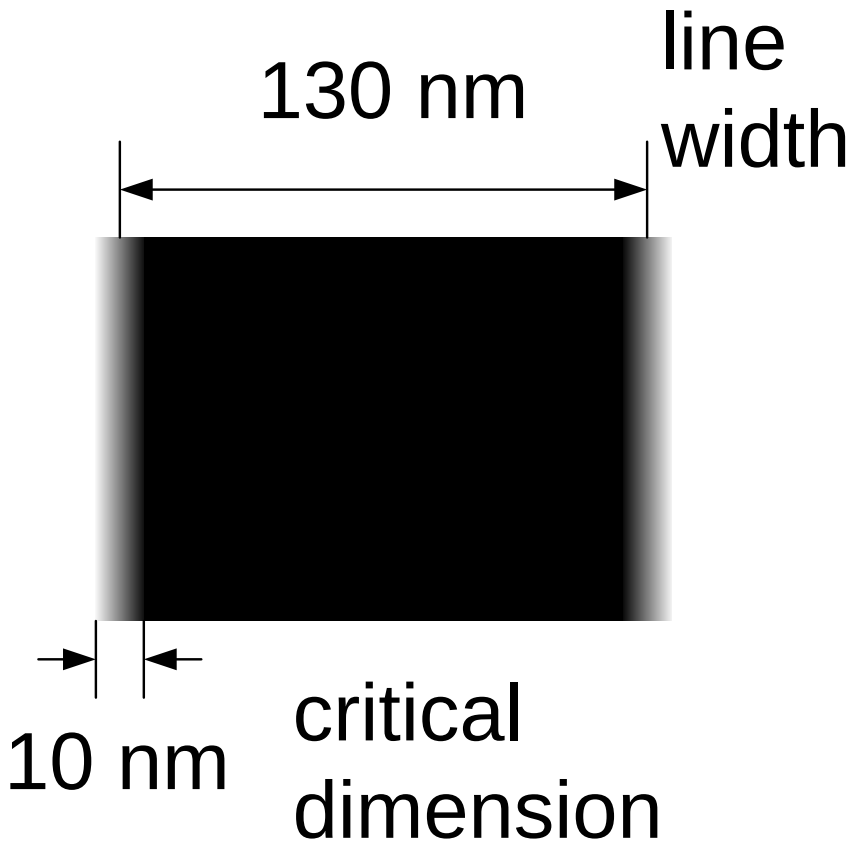
wafer

From stepping to scanning

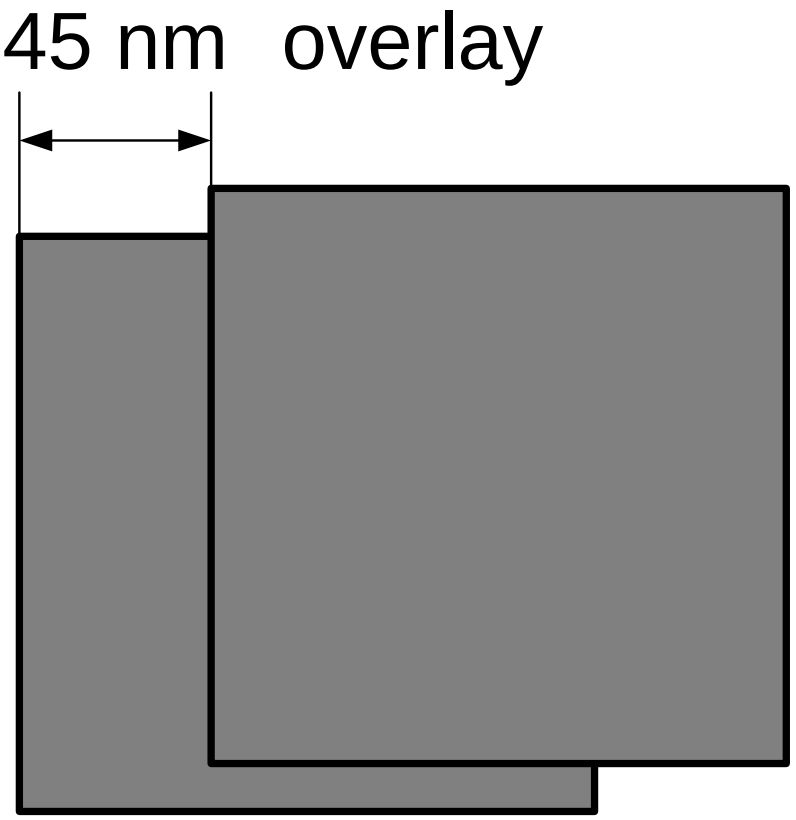


Key specifications waferstepper

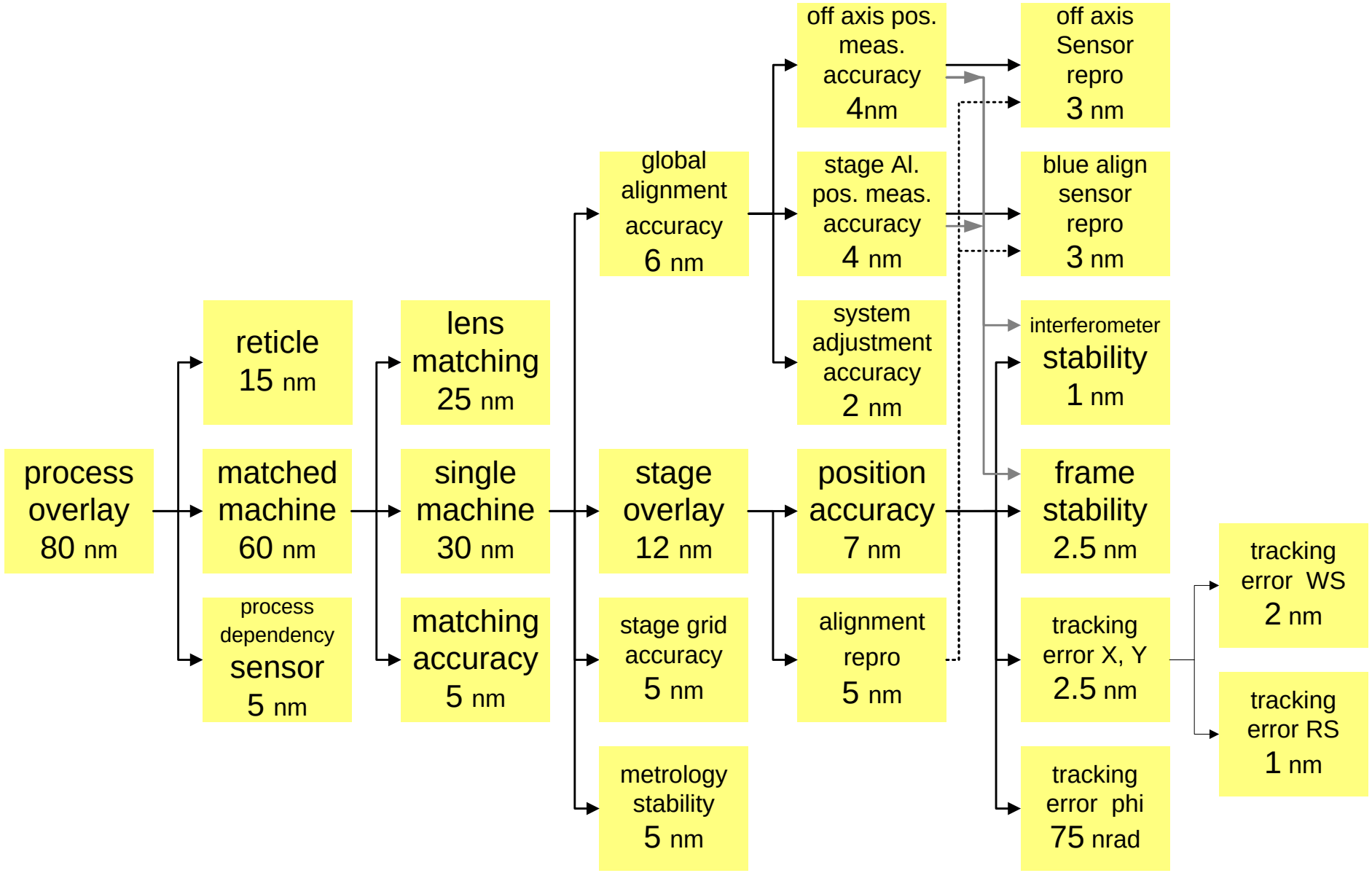
imaging



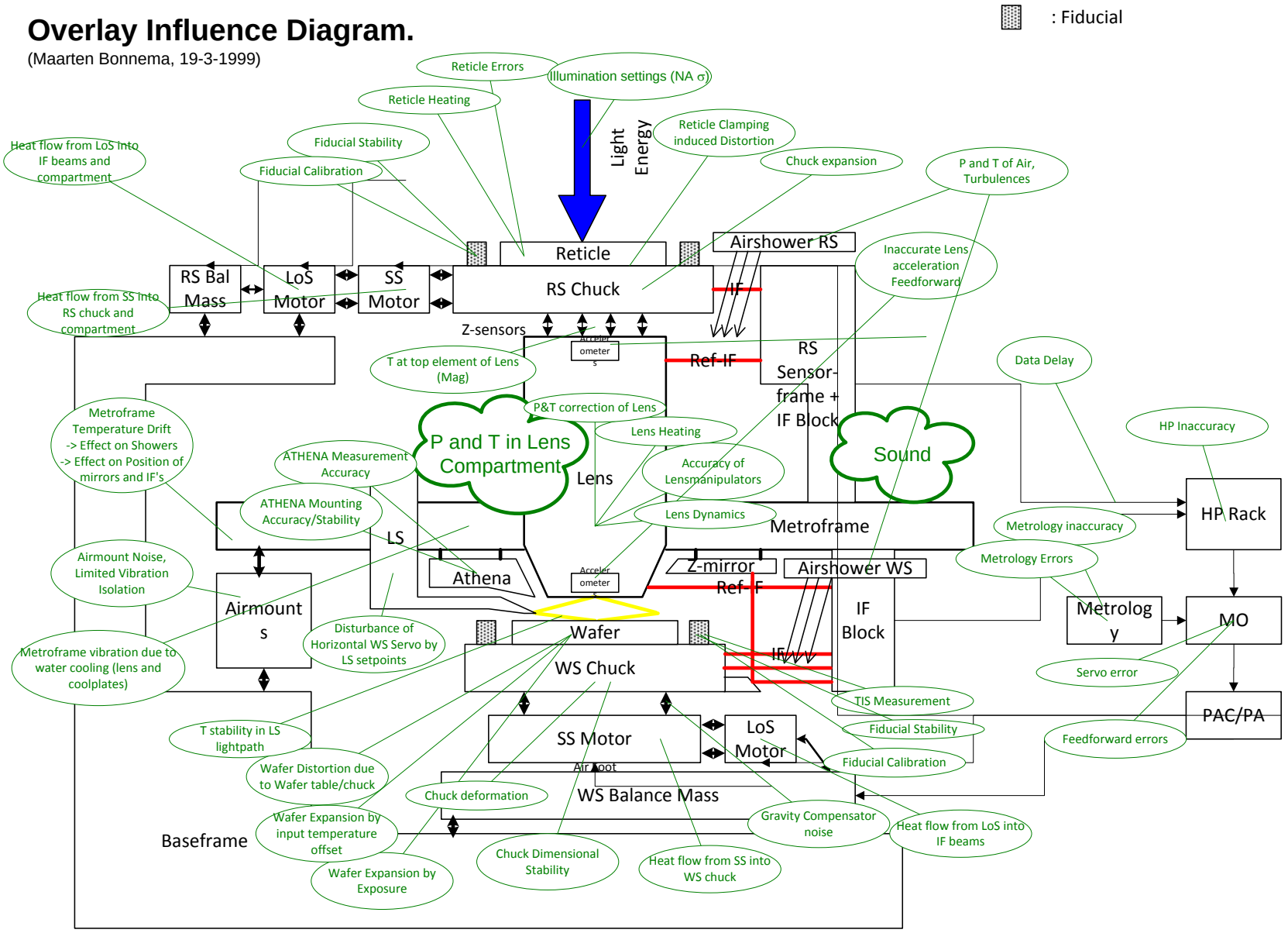
alignment



Overlay budget (1999)



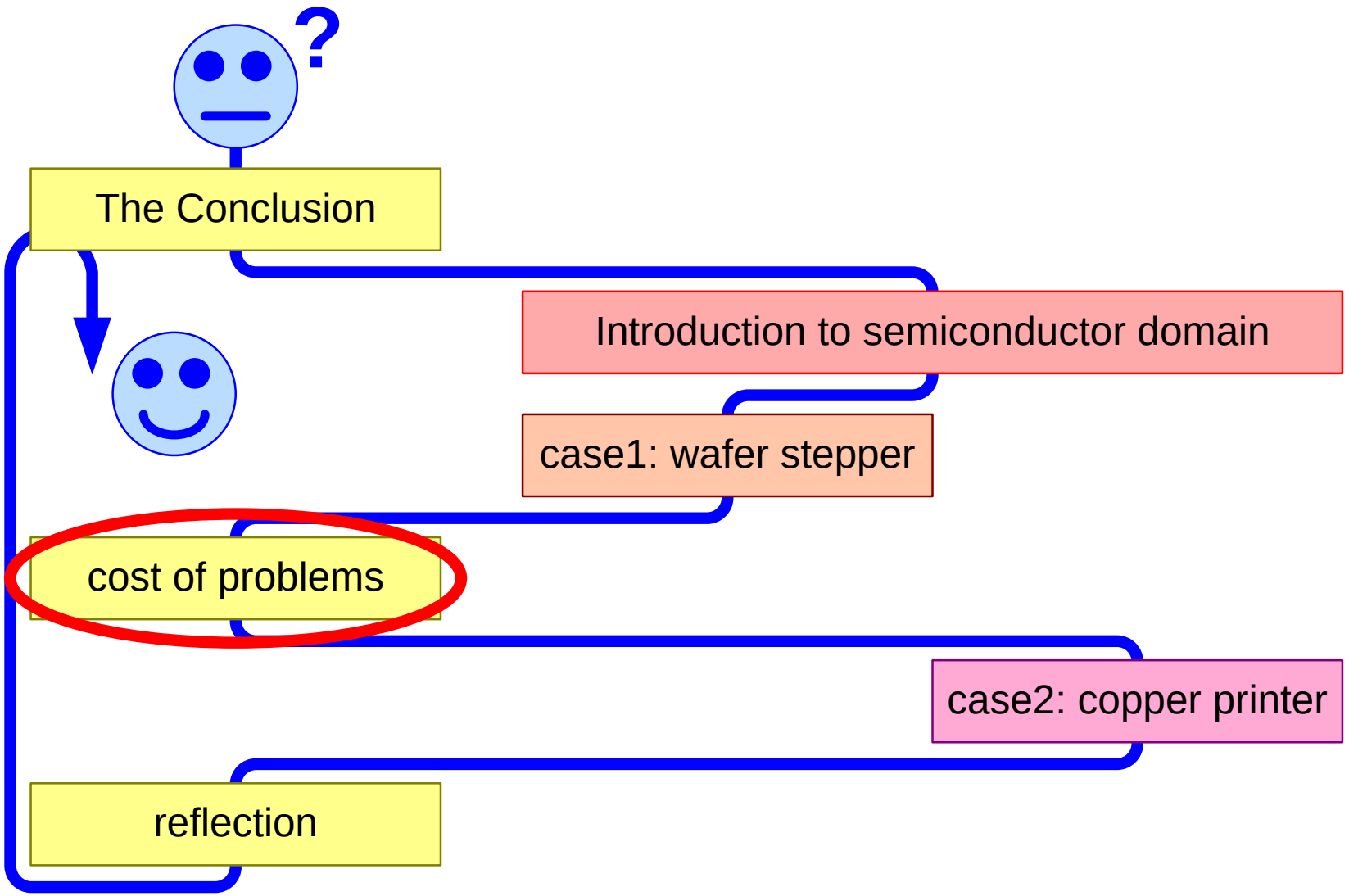
Everything influences overlay



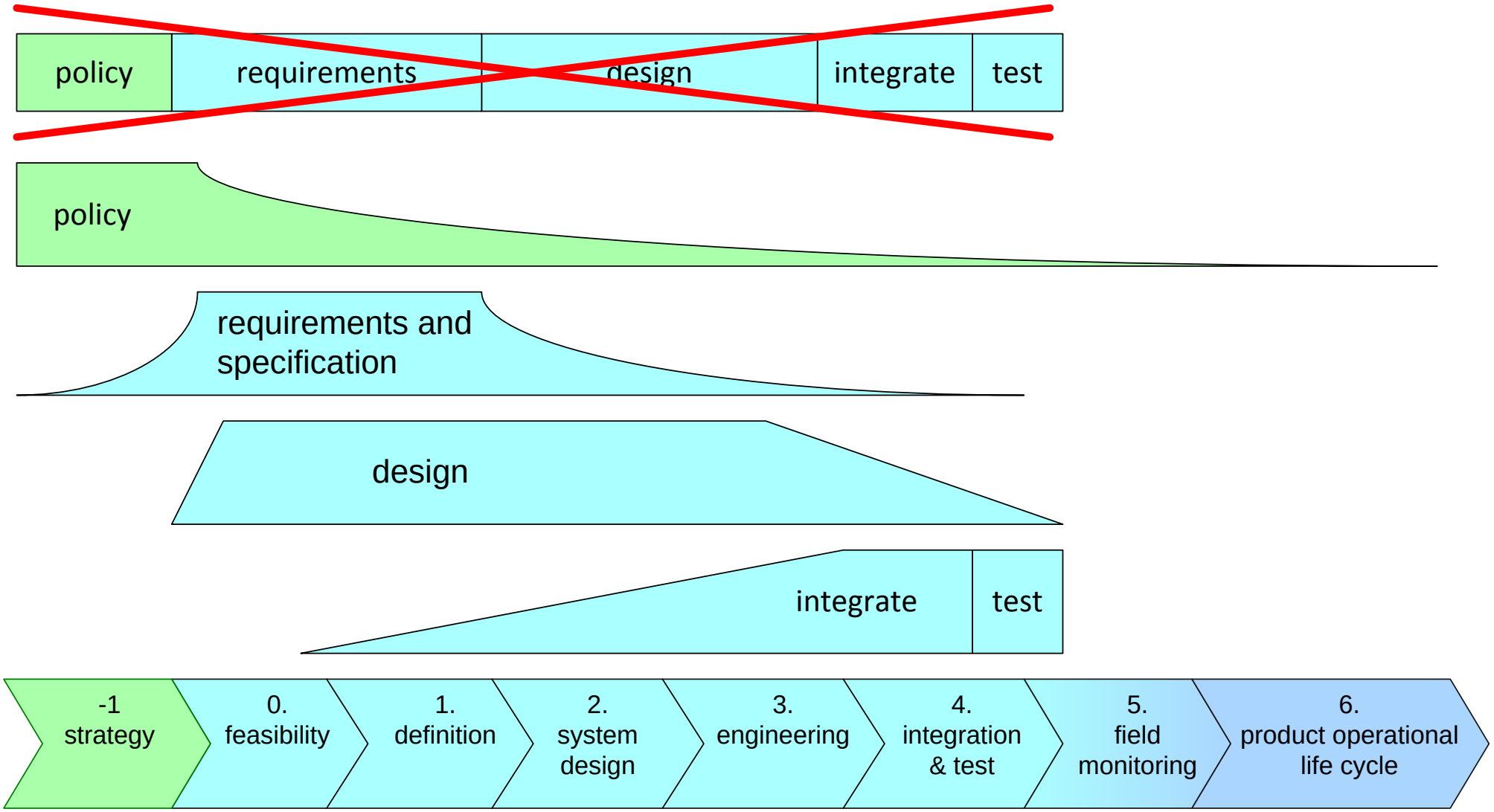
Integration of Overlay

test models for critical functions	build core machine	run manual sequence	expose
scanning stage	*stages, lens, alignment, level sensor, illumination*	*load wafer, align, focus, dose setting, and many more*	*process wafer measure overlay*

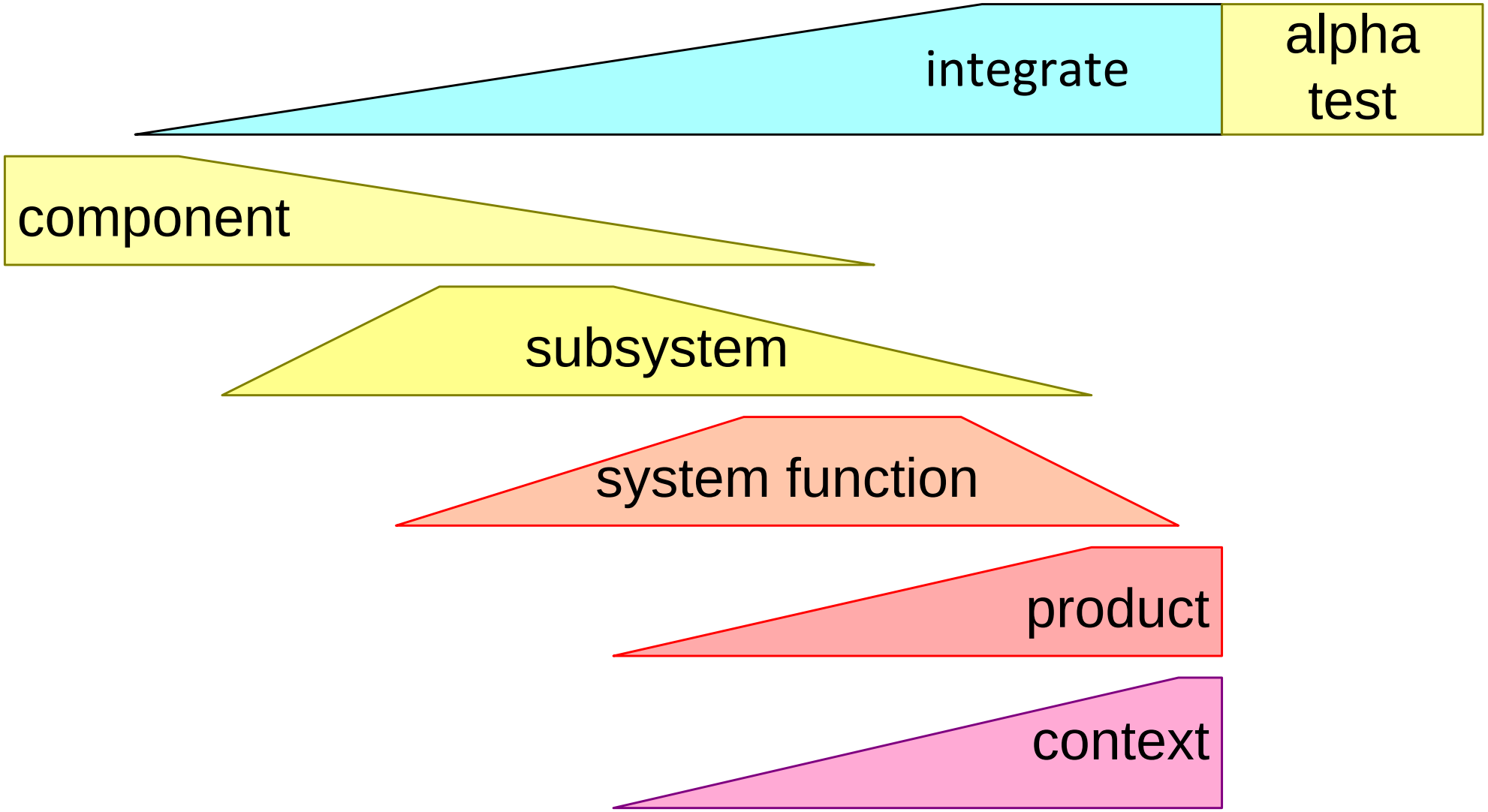
blood, sweat, and tears
trouble shooting
and learning


The Conclusion
Introduction to semiconductor domain
case1: wafer stepper
cost of problems
case2: copper printer
reflection

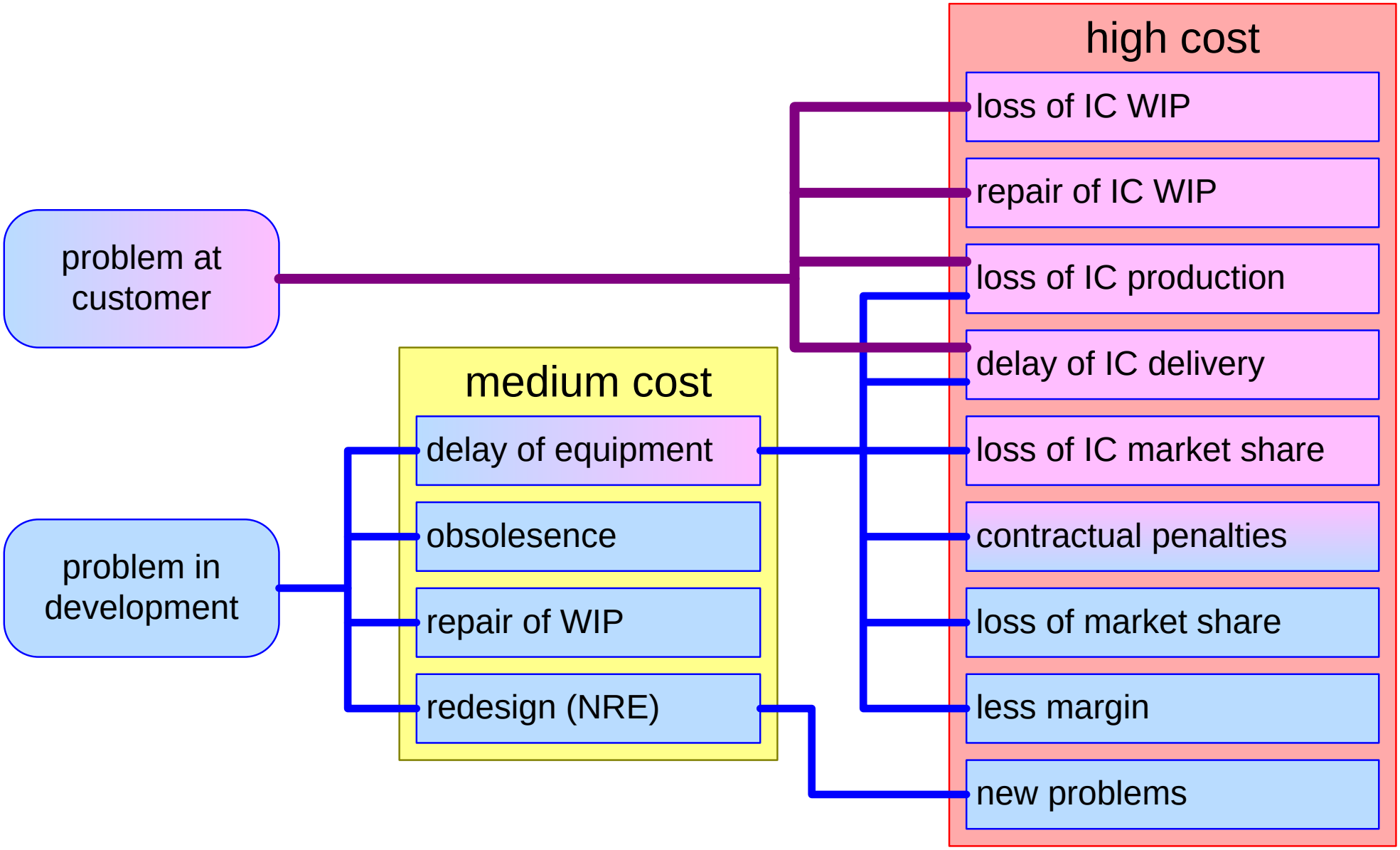
Typical Concurrent Product Creation Process



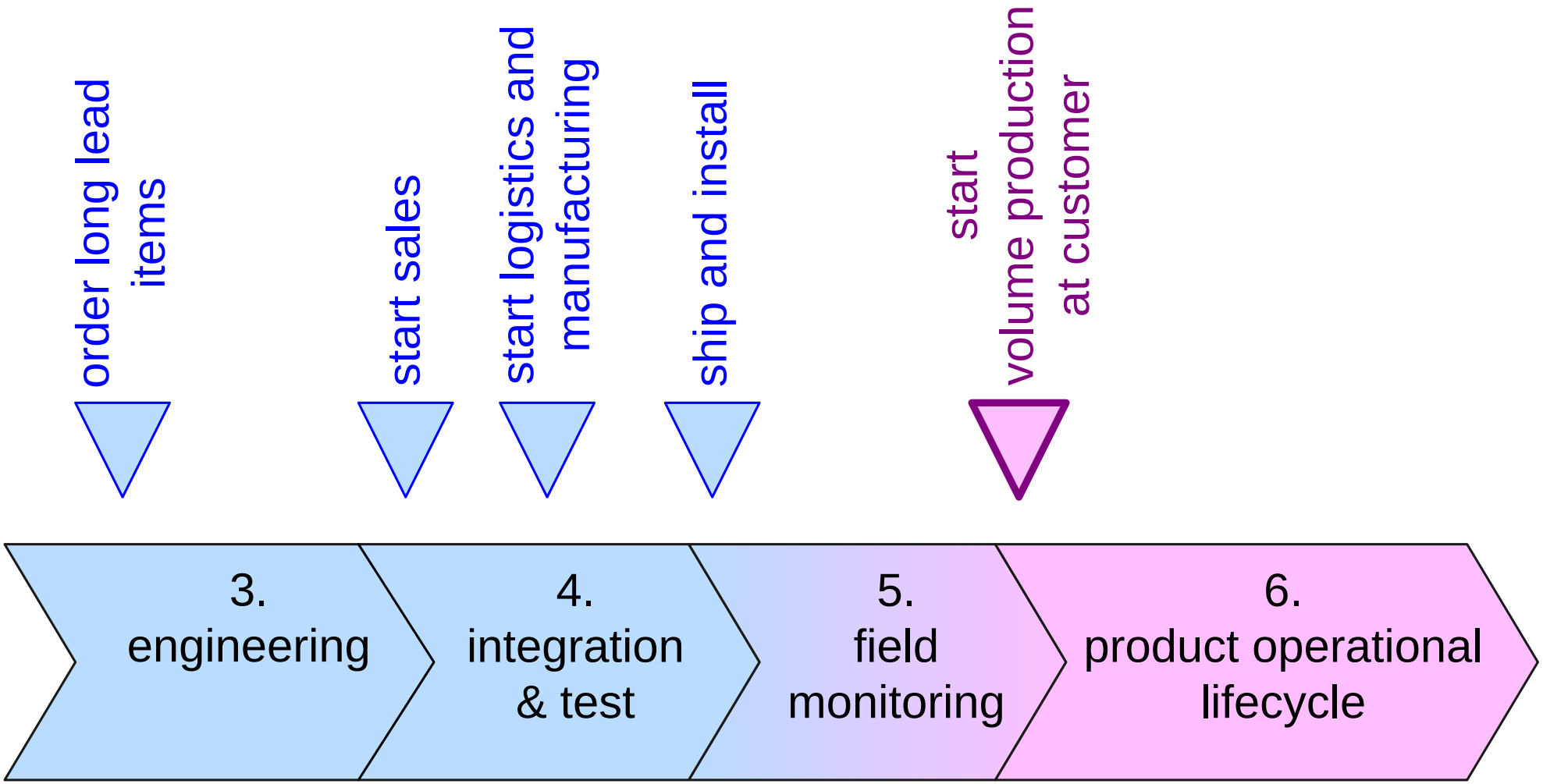
Integration Takes Place in a Bottom-up Fashion

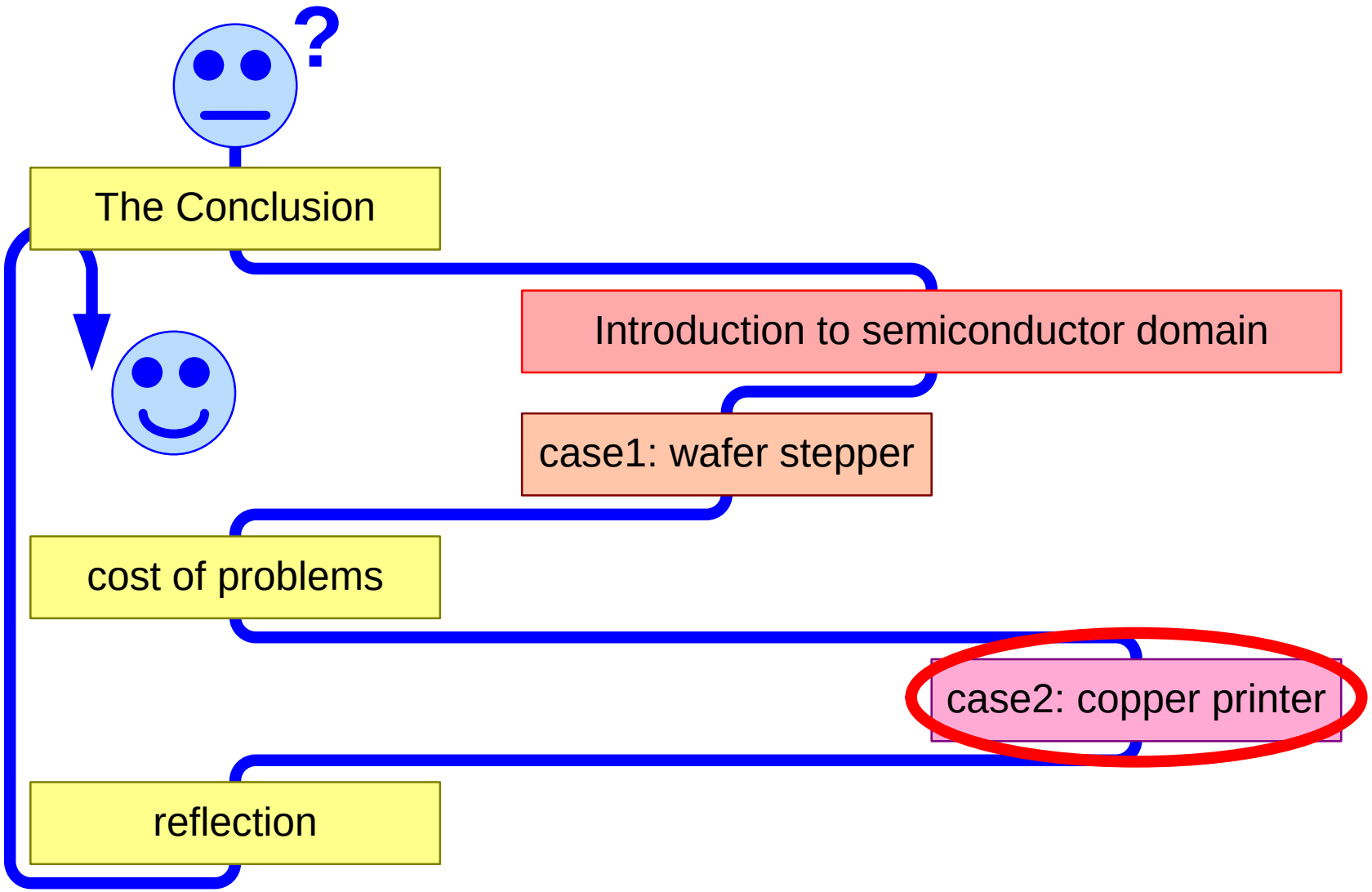


Costs of Encountered Problems

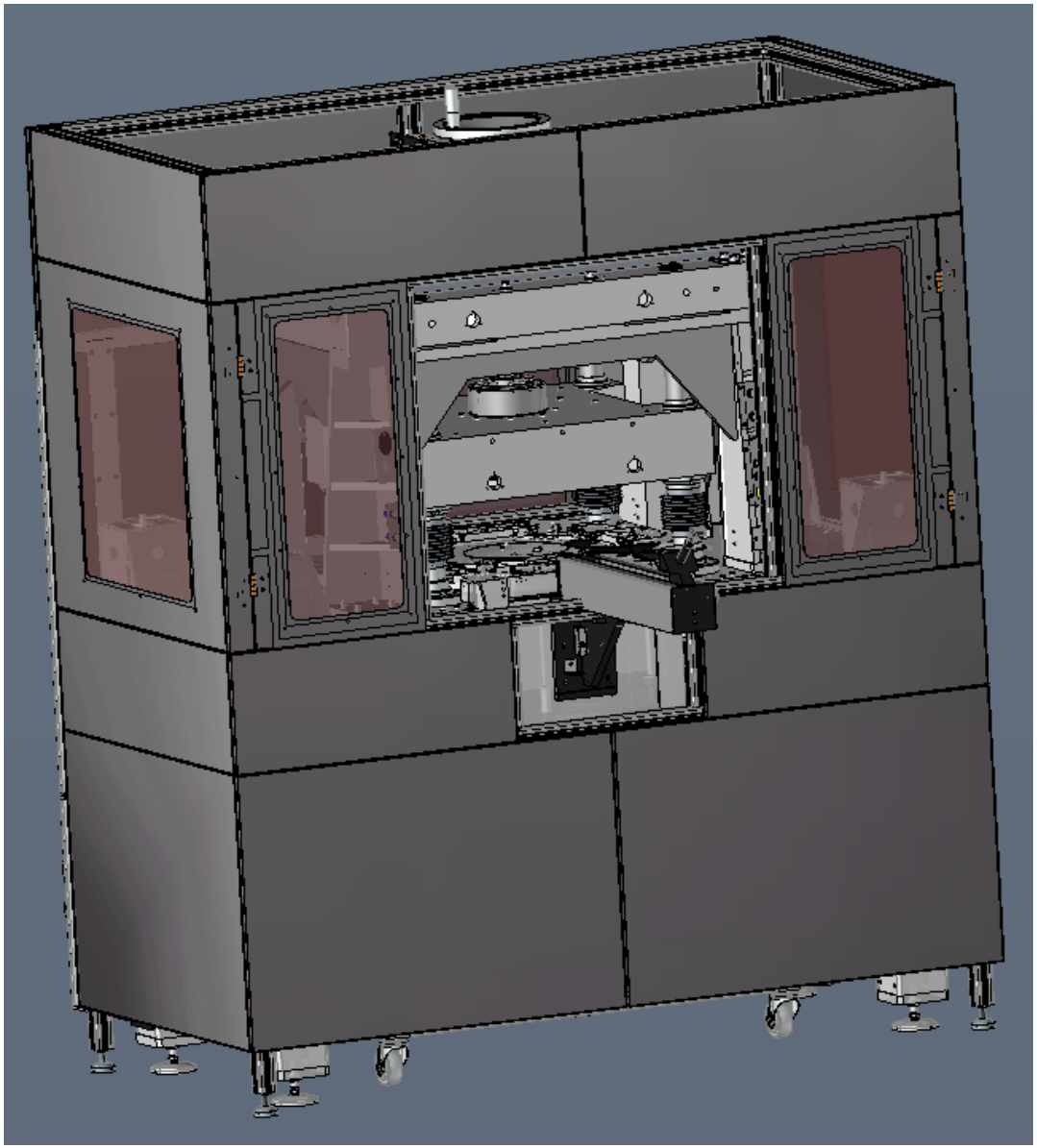


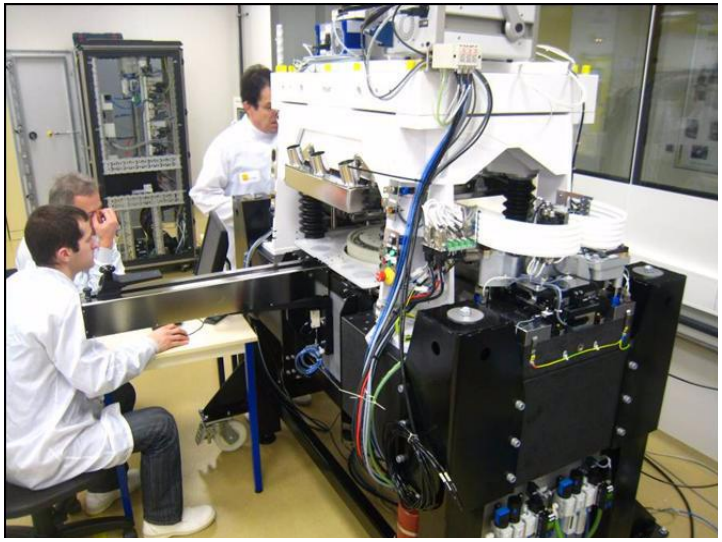
Cost Related Milestones



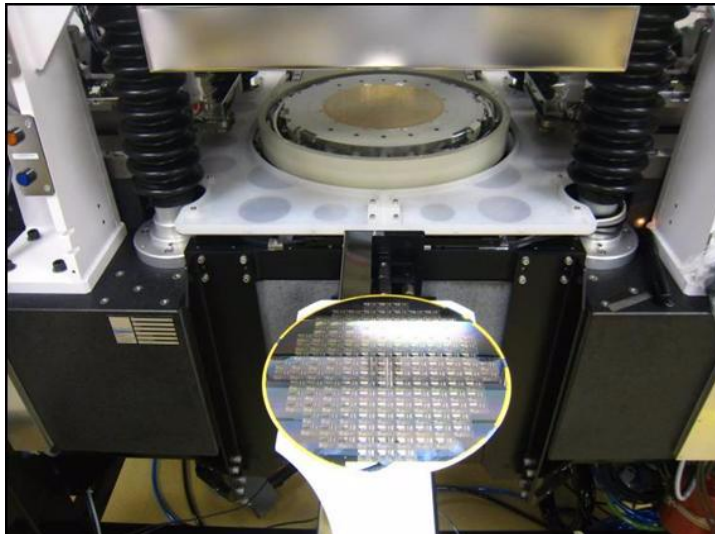

The Conclusion
Introduction to semiconductor domain
case1: wafer stepper
cost of problems
case2: copper printer
reflection

Case 2 Replisaurus Copper Printer

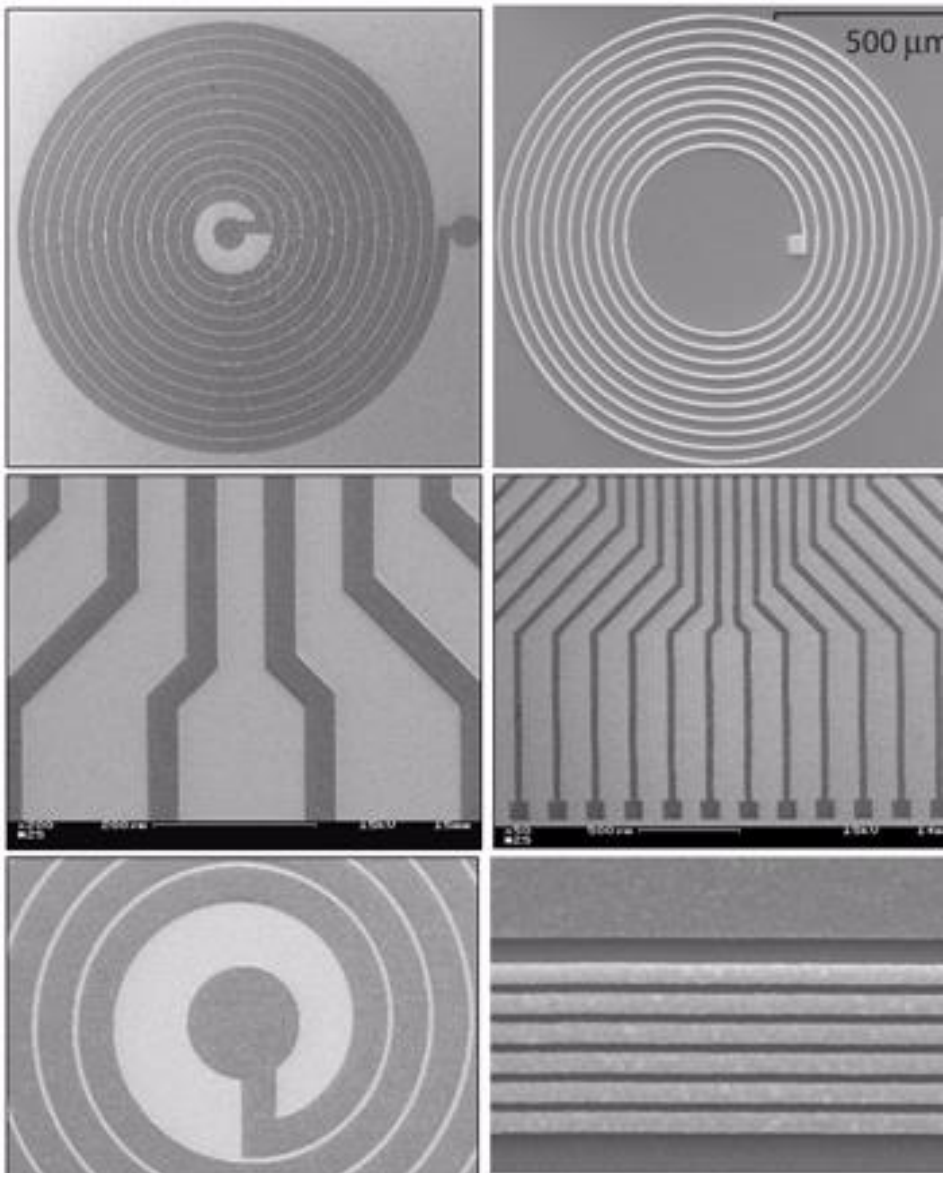




courtesy Replisaurus
www.replisaurus.com

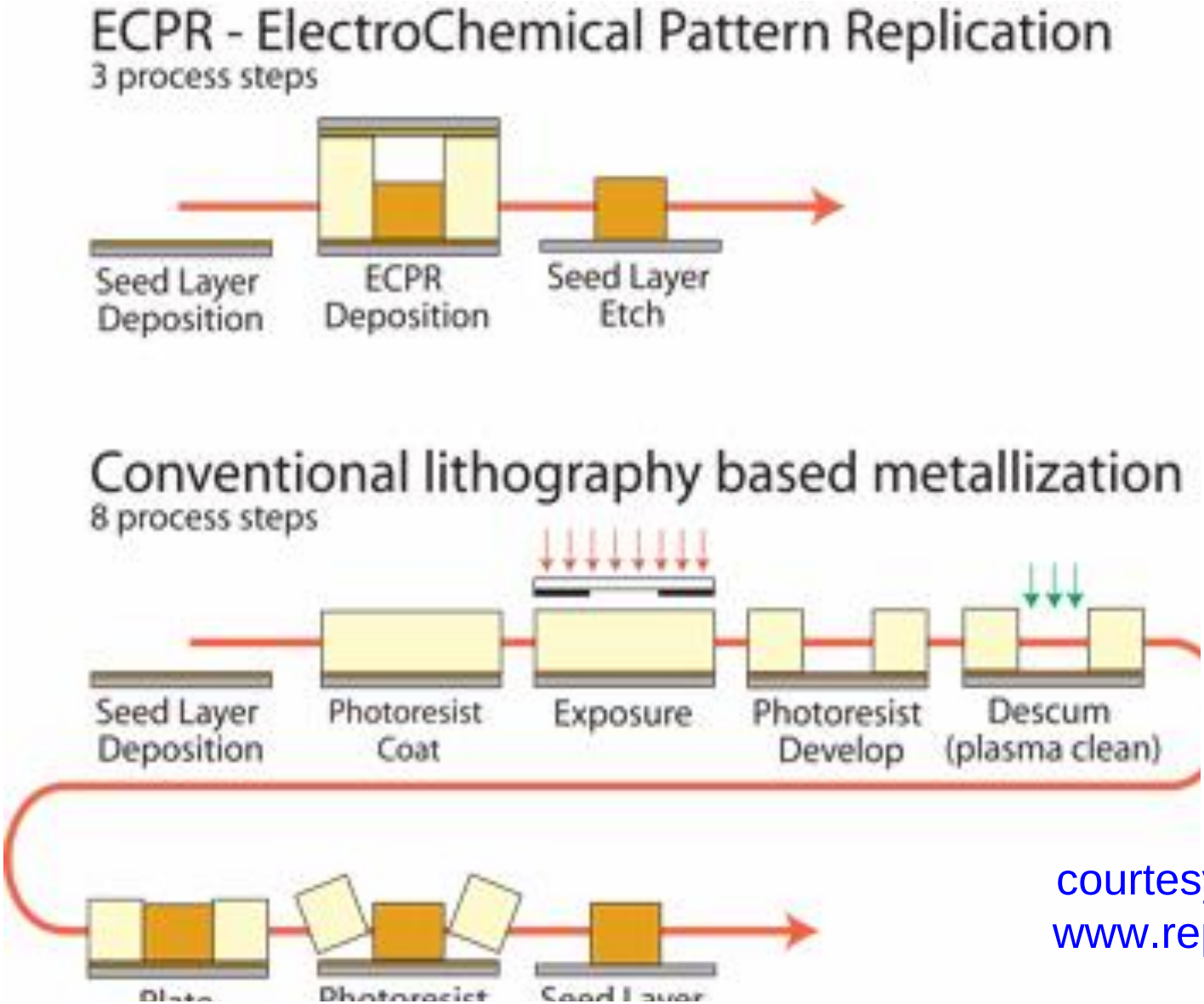


Example of printed copper structures



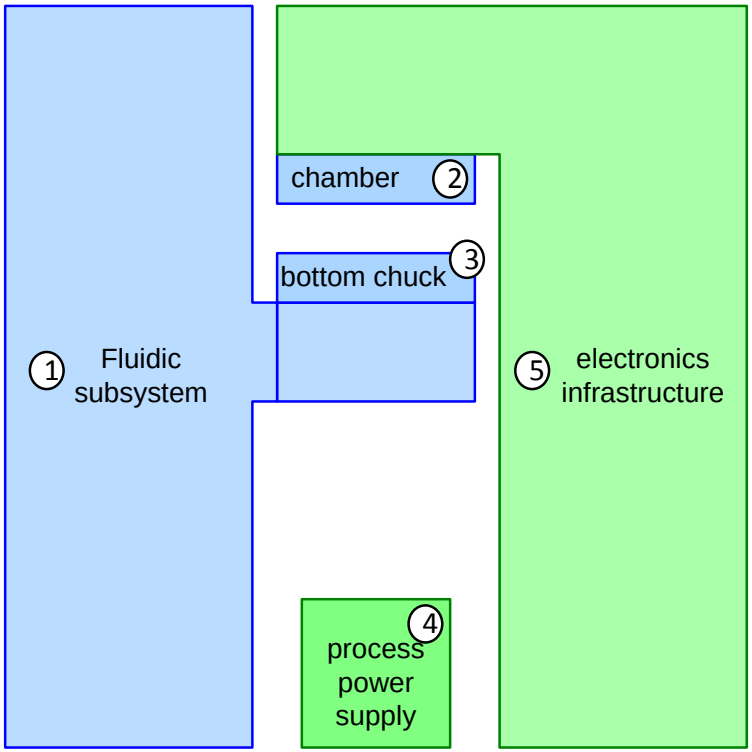
courtesy Replisaurus
www.replisaurus.com

ECPR technology replaces 6 process steps by 1 step

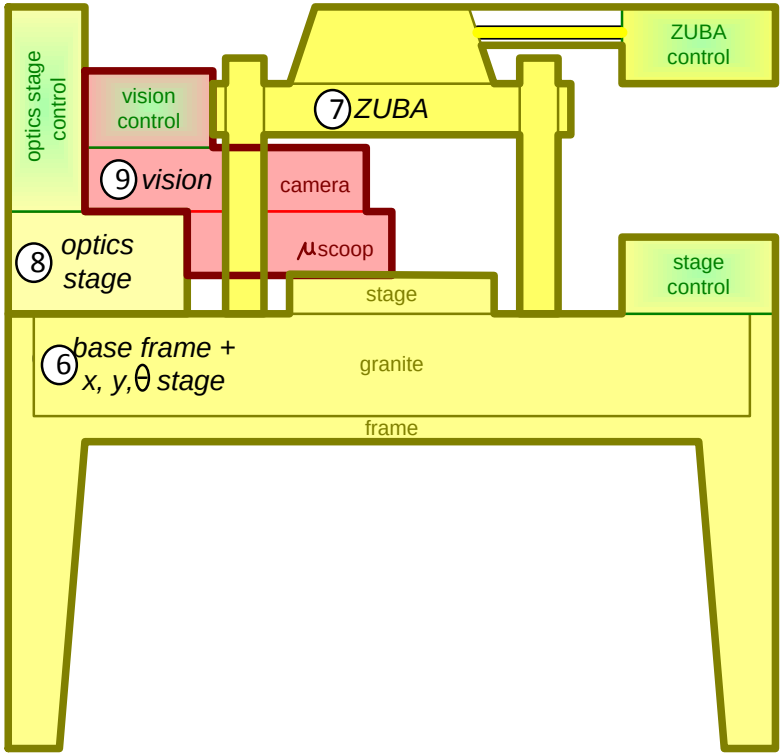


courtesy Replisaurus
www.replisaurus.com

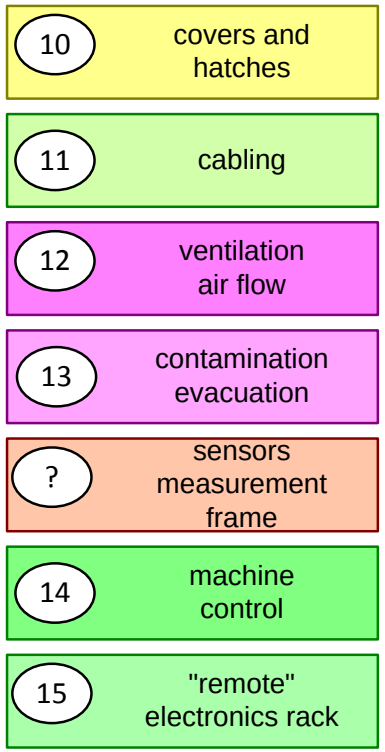
Decomposition in sub systems



back side view

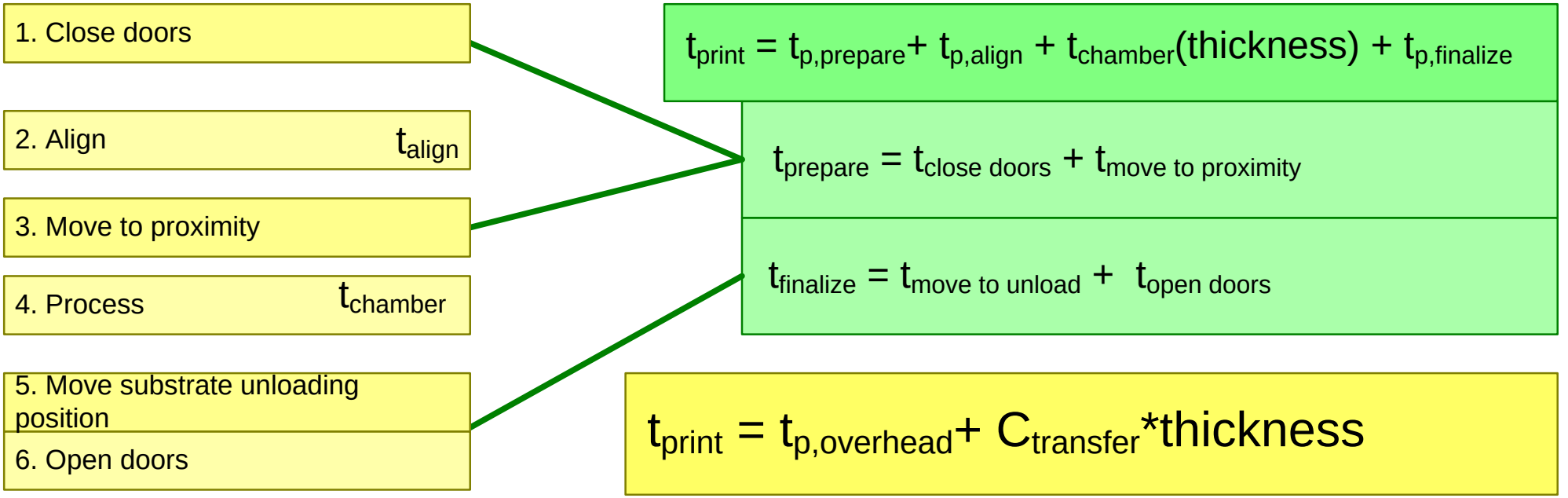


front side view



integrating

Ca. 2 days per quarter used for simple models

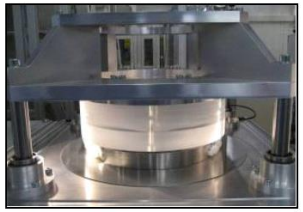


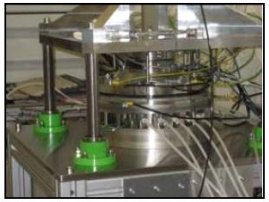
note: original diagram was annotated with actual performance figures for confidentiality reasons these numbers have been removed

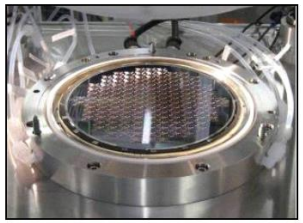
Continuous Modeling and Learning

200mm ECPR tools → **300mm ECPR tools**. Can be configured with 200 or 300mm kits.

2006 R&D 1.0

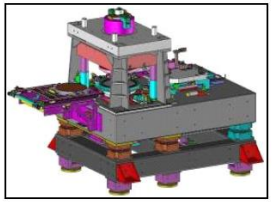


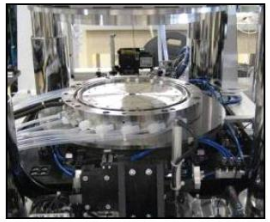




200mm hydraulic non-aligned tool for chamber & process development

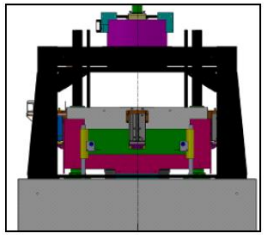
2007 REX 1.0

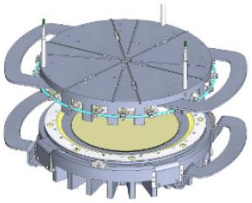




First aligned ECPR dev. tool. 200/300mm compatible.

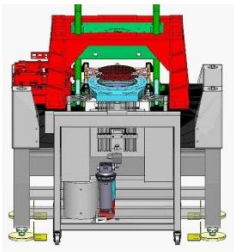
2008 R&D 2.0

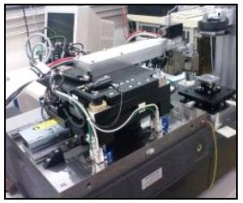


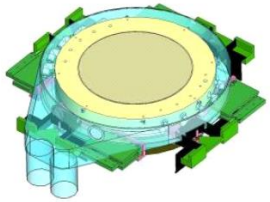


Integrated ECPR control. Non-aligned, Footprint, confinement

2009 REX 2.0

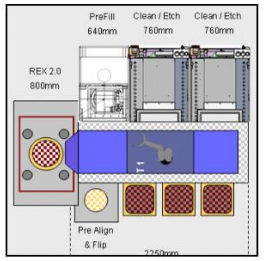


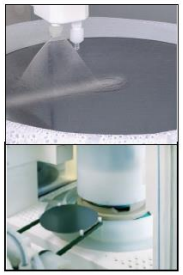


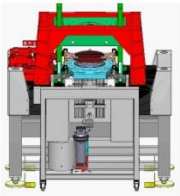


Production oriented print module. Cycle time, overlay, confinement & foot-print focus.

2010 Alpha 1.0

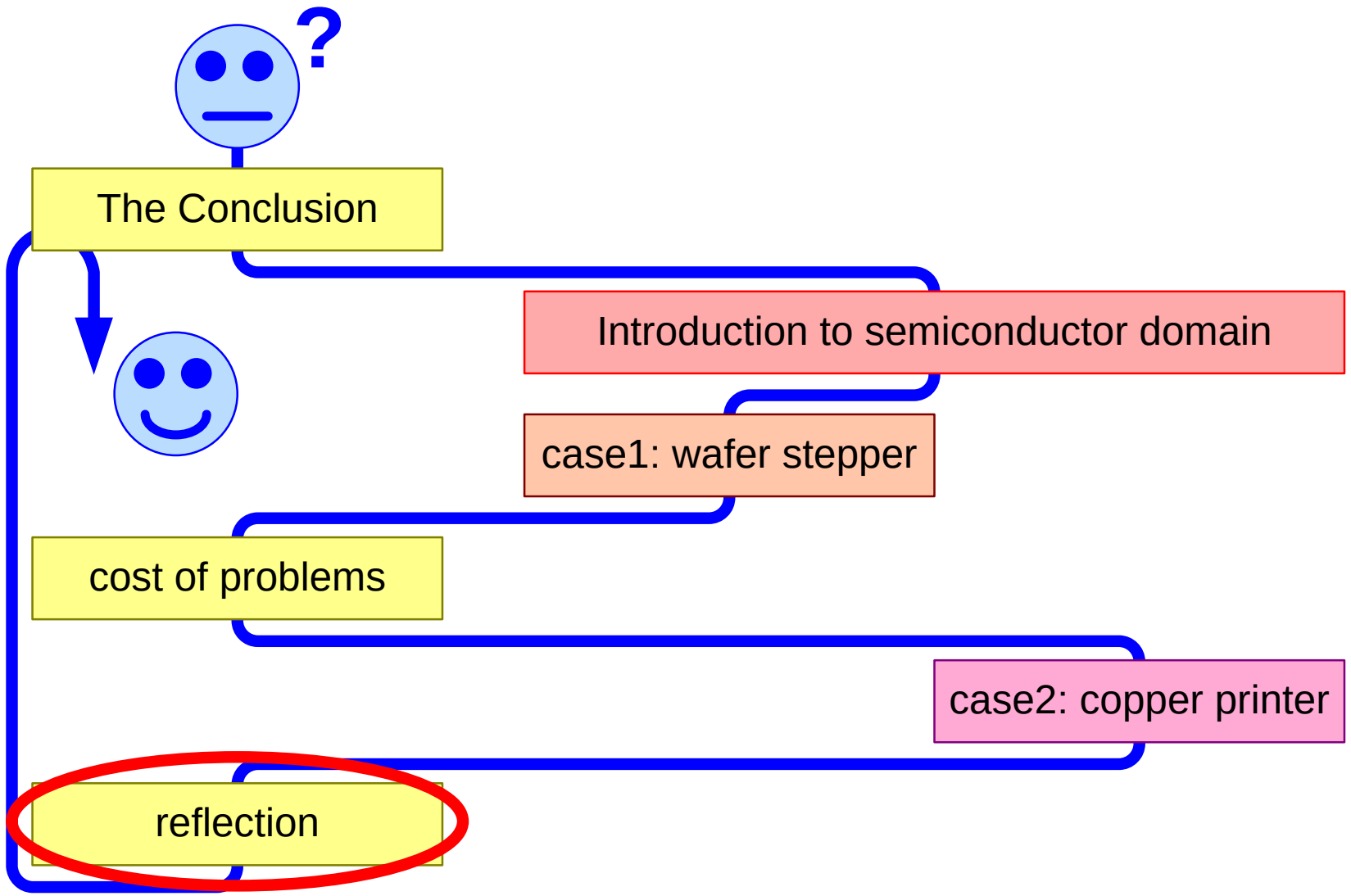






First integrated tool prefill – clean- print - seed etch.

courtesy Replisaurus


The Conclusion
Introduction to semiconductor domain
case1: wafer stepper
cost of problems
case2: copper printer
reflection

What We Teach:

functional decomposition

physical decomposition

modularity

interface management

seperation of concerns

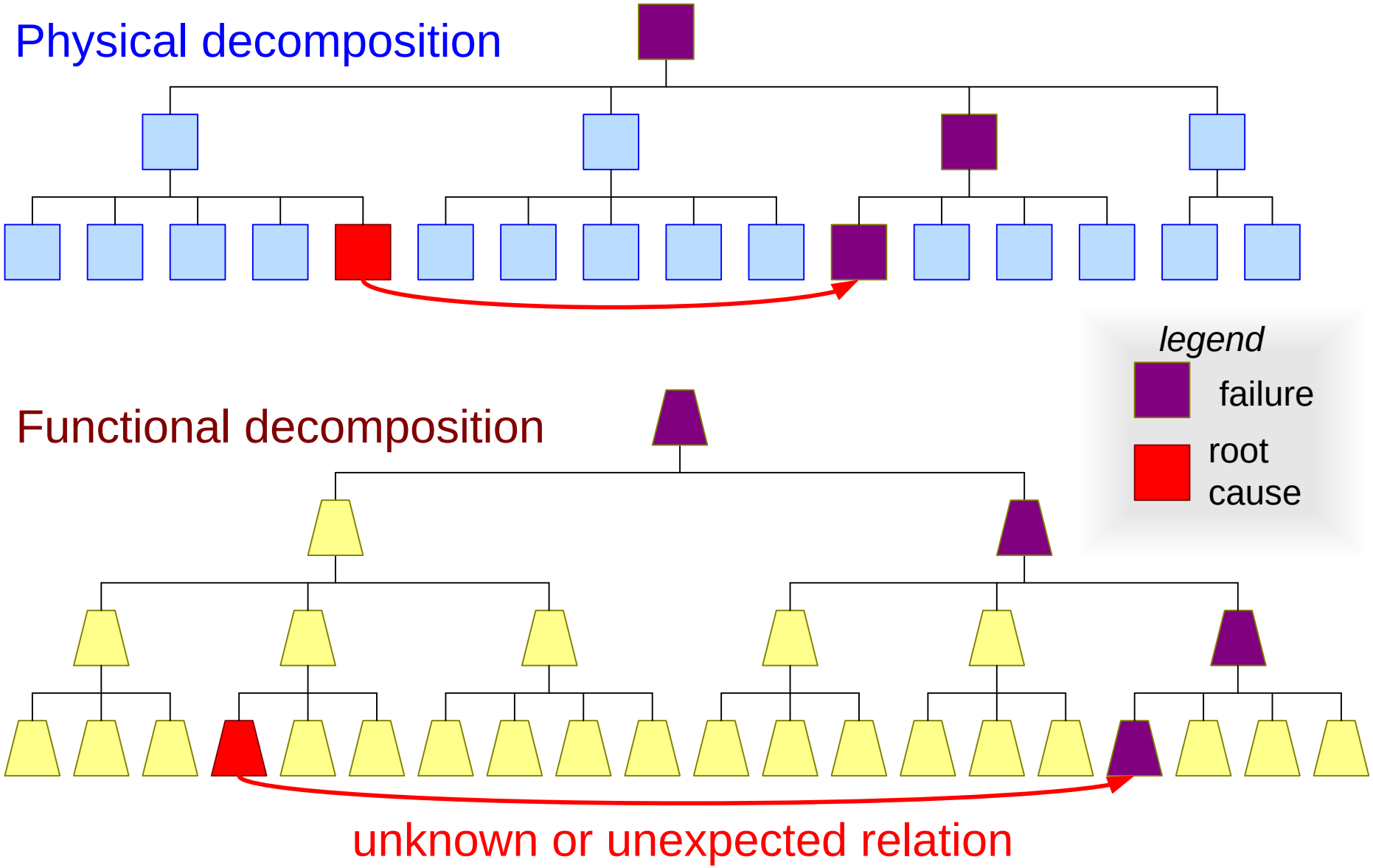
low coupling between components/functions

high cohesion within components/functions

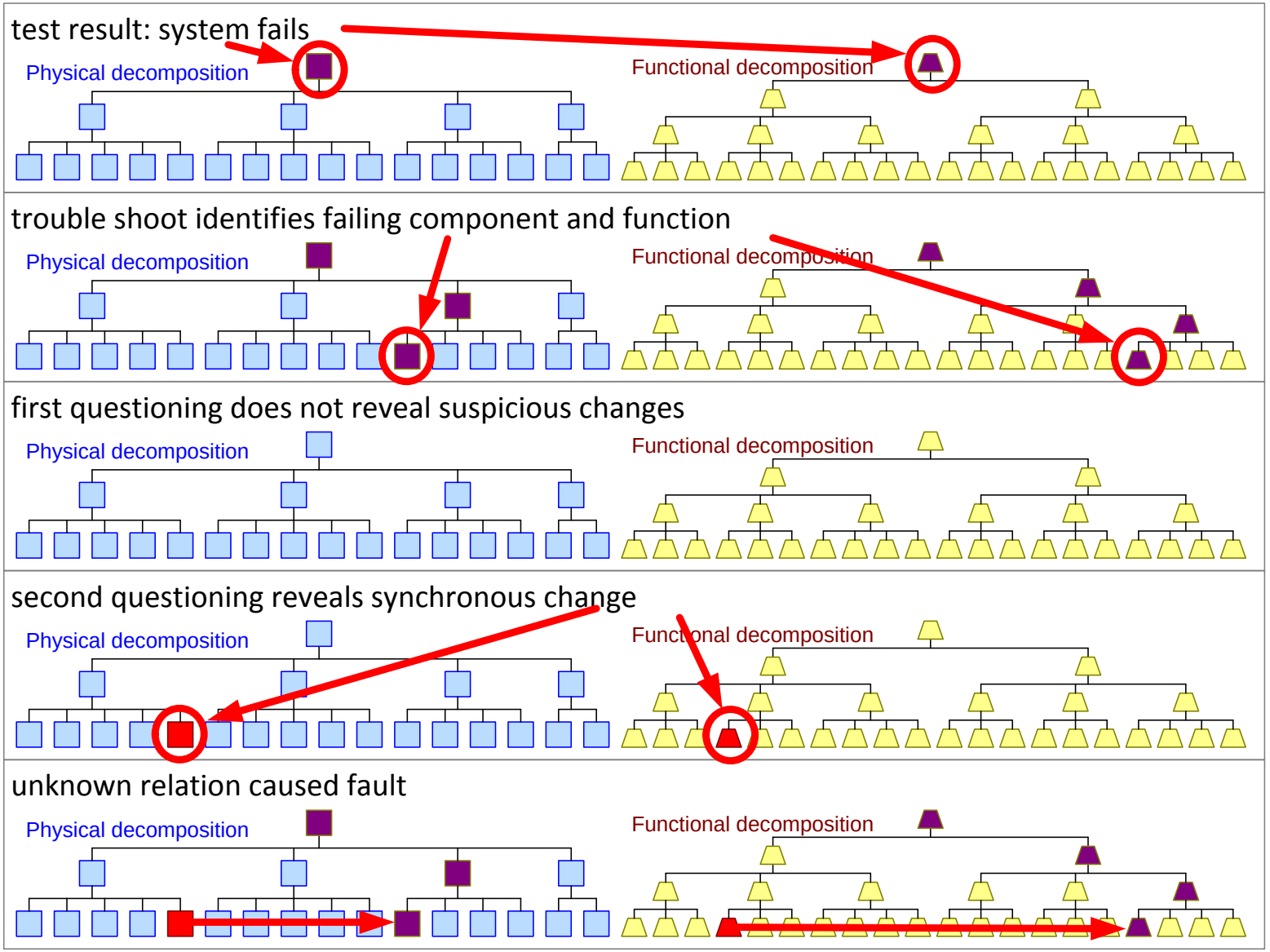
SMART (Specific, Measurable, ...)

traceability

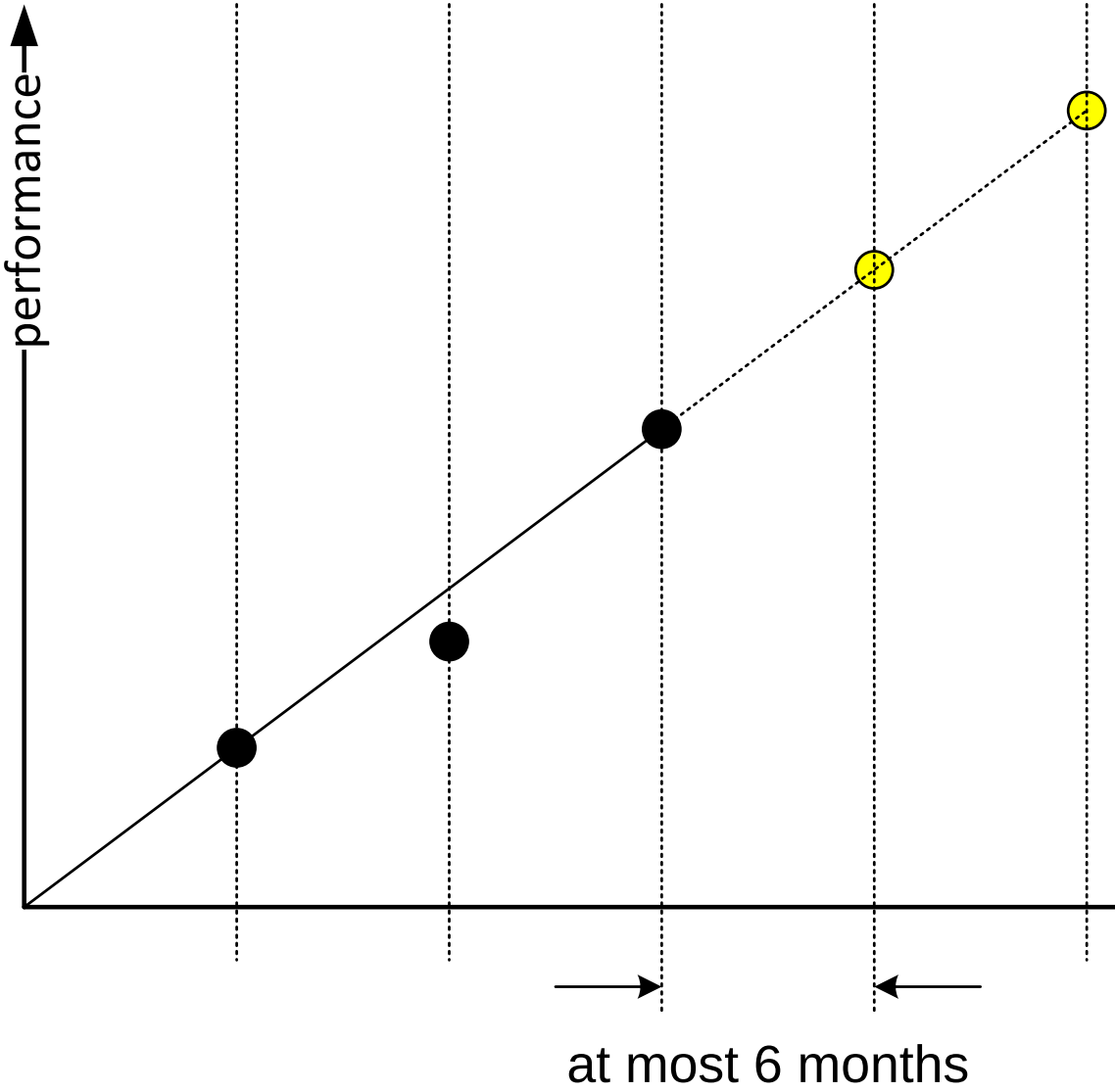
Root Cause is Often Elsewhere



“Nothing has been changed...”



Monitoring Performance Targets

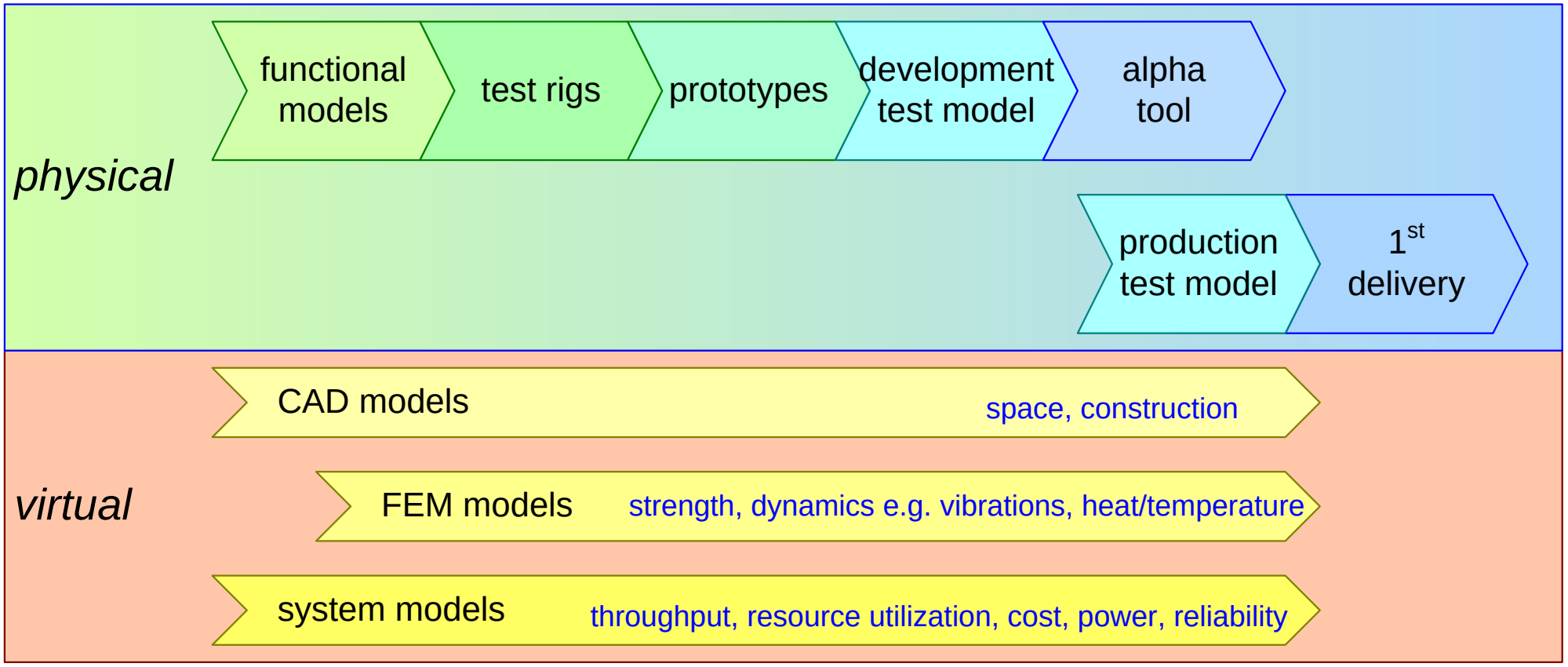


Weekly design meetings

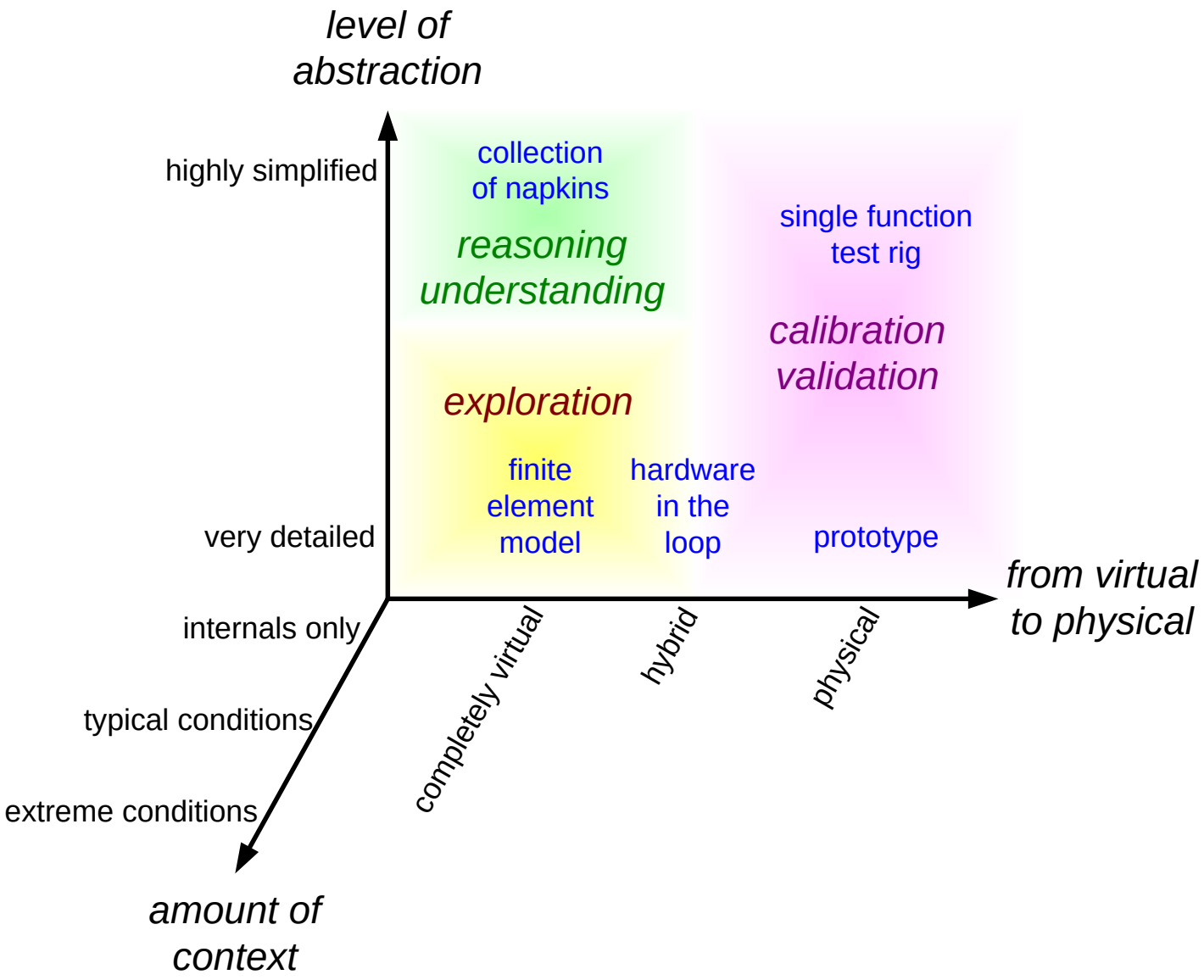
Bi monthly design reviews

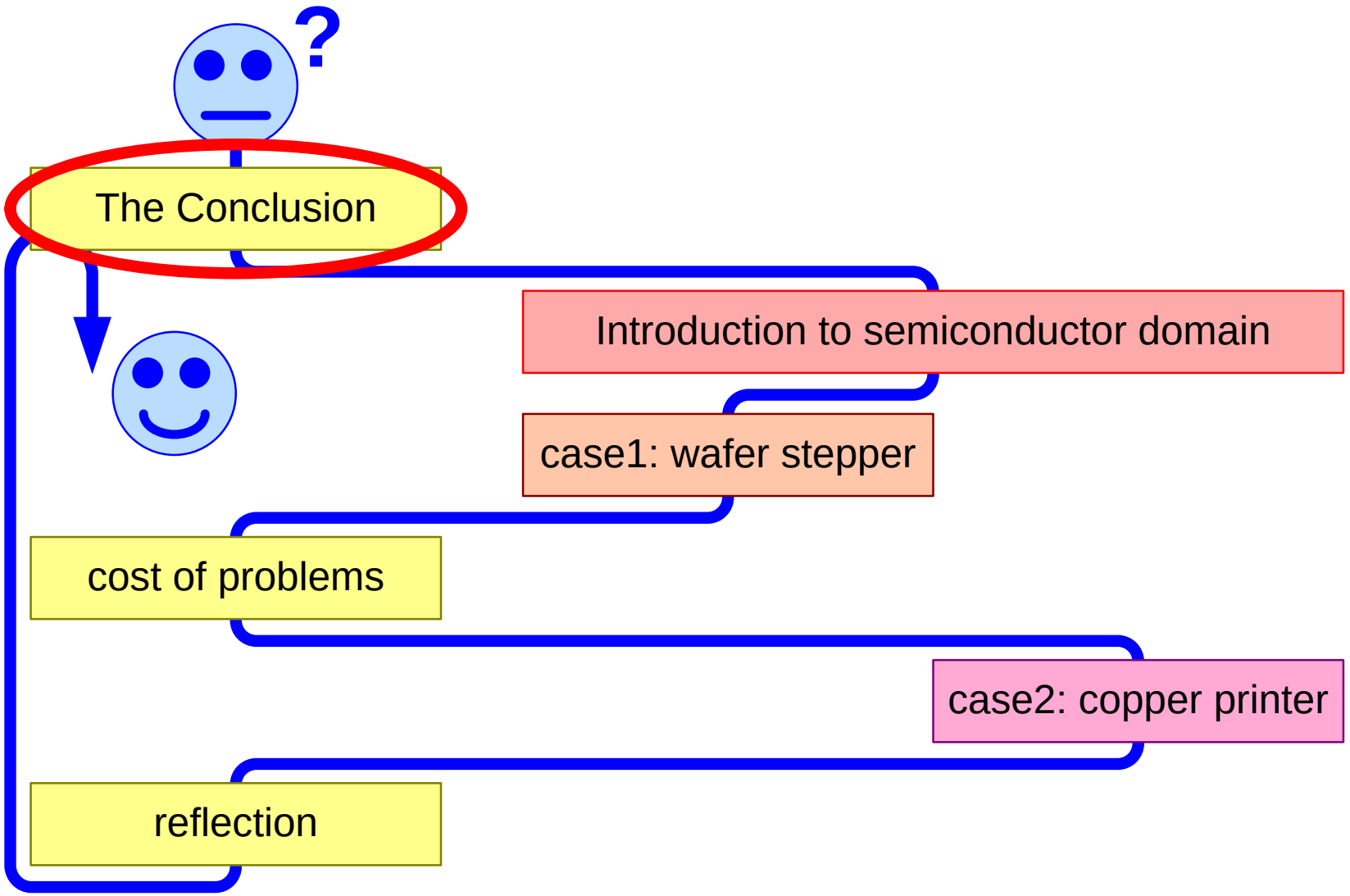
Half year milestones

Phasing of Models



Modeling Space




The Conclusion
Introduction to semiconductor domain
case1: wafer stepper
cost of problems
case2: copper printer
reflection

Conclusion from Semiconductor Cases

semiconductor domain conclusions

performance increase in semiconductor equipment is amazing

"bleeding edge": unforeseen, unknown, uncertain = normal

failing late = very costly

failing early = learning very fast

lessons for other domains

other domains with increasing innovation rate (decreasing time-to-market) will get more unforeseen, unknown, uncertain issues

failing early is always better than failing late

The Final Conclusion

Early ***investments*** in

test rigs, prototypes, virtual models, and simulations

save a lot of money