#### Execution architecture concepts

by Gerrit Muller University of South-Eastern Norway-NISE e-mail: gaudisite@gmail.com www.gaudisite.nl

#### Abstract

The execution architecture determines largely the realtime and performance behavior of a system. Hard real time is characterized as "missing a deadline" will result in system failure, while soft real time will result "only" in dissatisfaction. An incremental design approach is described. Concepts such as latency, response time and throughput are illustrated. Design considerations and recommendations are given such as separation of concerns, understandability and granularity. The use of budgets for design and feedback is discussed.

#### Distribution

This article or presentation is written as part of the Gaudí project. The Gaudí project philosophy is to improve by obtaining frequent feedback. Frequent feedback is pursued by an open creation process. This document is published as intermediate or nearly mature version to get feedback. Further distribution is allowed as long as the document remains complete and unchanged.

August 21, 2020 status: preliminary draft version: 1.1



#### Execution Architecture





hard real time		soft real time		
disastrous failure		dissatisfaction		
human device lo safety safety fund	oss of ctionality	limited throughput	waiting time	
loss of information coordin		s of hand ination		



## Smartening requirements



Well defined set of performance critical cases



Typical within desired time, limited exceptions allowed.

Exceptions may not result in functional failure











# Throughput



# throughput:

- + processing steps/frame
- + frames/second
- + concurrent streams



## Gross versus Nett

bus bandwidth, processor load [memory usage] useful macroscopic views, be aware of microscopic behavior





#### Design recommendations separation of concerns



#### Design recommendations understandability





# Granularity considerations



coarse grain:
rigid
low overhead



#### synchronous

safety critical, reliable, subsystems

very low overhead predictable understandable

works best in total separation does not work for multiple rhythms

#### thread based

Asynchronous applications and services

separation of timing concerns sharing of resources (no wait)

poor understanding of concurrency danger of high overhead

timer based

regular rhythm;

low "tunable" overhead understandable

fast rhythms significant overhead



I/O and HW events

separation of timing concerns

definition of interrupts determines: overhead, understandability



## Synchronous design





double buffer:

full decoupling of calculation and execution



## Actual timing on logarithmic scale





#### Typical micro benchmarks for timing aspects

	infrequent operations, often time-intensive	often repeated operations
database	start session finish session	perform transaction query
network, I/O	open connection close connection	transfer data
high level construction	component creation component destruction	method invocation same scope other context
low level construction	object creation object destruction	method invocation
basic programming	memory allocation memory free	function call loop overhead basic operations (add, mul, load, store)
OS	task, thread creation	task switch interrupt response
HW	power up, power down boot	cache flush Iow level data transfer



# The transfer time as function of blocksize





# Example of a memory budget

memory budget in Mbytes	code	obj data	bulk data	total
shared code User Interface process database server print server optical storage server communication server UNIX commands compute server	11.0 0.3 0.3 0.3 0.3 0.3 0.3 0.3	3.0 3.2 1.2 2.0 2.0 0.2 0.5	12.0 3.0 9.0 1.0 4.0 0 6.0	11.0 15.3 6.5 10.5 3.3 6.3 0.5 6.8
system monitor	0.3	0.5	0	0.8
application SW total	13.4	12.6	35.0	61.0
UNIX Solaris 2.x file cache				10.0 3.0
total				74.0



complications measures considered margin cache explicit behavior bus allocation architecture rules memory management monitoring, logging garbage collection pool management memory (buffer, storage) fragmentation feedback to architect non preemptable OS activities flipover simulation "hidden" dependencies (ie [dead]locks) systematic "coincidences", avalanche triggers instable response, performance

