

# The Waferstepper Challenge: Innovation and Reliability despite Complexity



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## Abstract

The function of the waferstepper is explained and its most important characteristics. The dynamic market provides continuous technological challenges, resulting in ever increasing performance, but also complexity. Despite the exponential increase of performance and complexity, the reliability must be good. The reliability is crucial when the stepper is used in volume production.

The ASML engineering style plays a central role in tackling this challenge. Three key aspects of this style are: Feedback, Focus and Future awareness. The concurrent application of these three aspects has so far been proven to be effective.

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### disclaimer

The case material is based on actual data, from a complex context with large commercial interests. The material is **simplified** to increase the accessibility, while at the same time **small changes** have been made to remove commercial sensitivity. Commercial sensitivity is further reduced by using relatively **old** data (between 5 and 10 years in the past). Care has been taken that the illustrative value is maintained

## 1 Introduction

ASML builds wafersteppers, lithography equipment used by semiconductor manufacturers. The lithography equipment determines to a high degree the performance and cost of the semiconductor manufacturing.



Figure 1: ASML Twinscan AT1100

Figure 1 shows one of the most recent ASML products, the Twinscan AT1100. This is an 193nm high NA scanner, capable of handling 300 mm wafers.

The main function of the waferstepper is to "print" the electronic circuit information on the wafer. The waferstepper is only exposing the wafer, the actual circuit

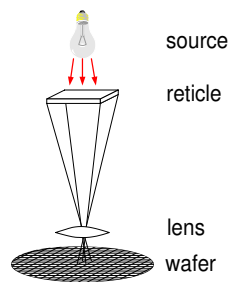


Figure 2: What is a waferstepper

is formed by many processing steps in the semiconductor fab. Many (typical hundreds) dies, identical electronic circuits, fit on one wafer. A few dies are exposed at a time. The original information for the exposure resides on the mask or reticle. This mask or reticle is 4 or 5 times larger than the final circuitry. Via an extremely high quality, but expensive lens subsystem the original is projected on the wafer, see figure 2.

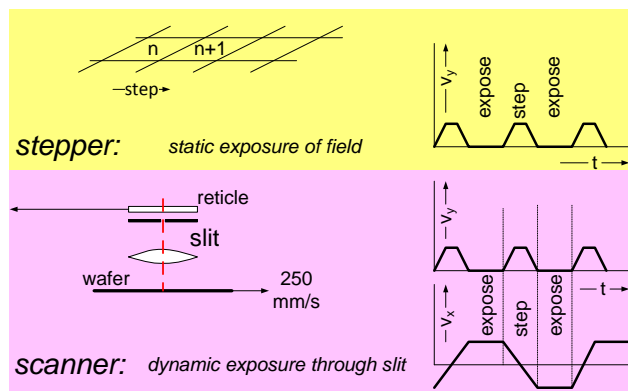


Figure 3: From stepping to scanning

Modern wafersteppers actually do the exposure scanwise, where both reticle and wafer move and the light is passing through a narrow slit, see figure 3. Scanning is using the lens more effectively than static exposure of the entire area.

Lithography customers use a few key specifications for the lithography operation, see also figure 4:

- Critical Dimension (CD) control or imaging
- Overlay

The Critical Dimension (CD) control defines how accurate the linewidth of

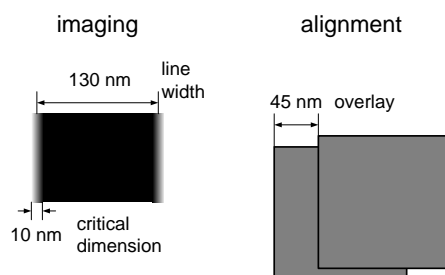


Figure 4: Key specifications waferstepper

structures can be controlled. This parameter strongly influences the final performance (speed, power) of the electronic circuitry.

The overlay is defined as the repositioning accuracy of successive exposures. Electronic circuitry is build by exposing and processing layer by layer. Hence the same wafer is exposed many times, with days to weeks in between, where the next layer must be at (nearly) the same position. The overlay amongst others strongly influences the density of electronic components that can be obtained.

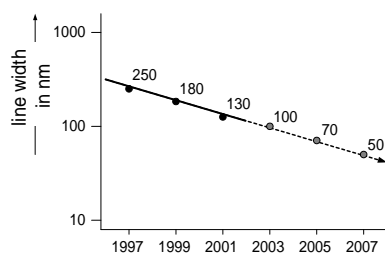


Figure 5: Moore's law

The entire semiconductor industry is driven by Moore's law, see the visualization in figure 5. Most competitors try to leapfrog each other by being faster than Moore's law, creating an extremely competitive environment, with large stakes.

In order to achieve the required performance figures technical budgets are used, see figure 6. Such a budget is a decomposition of the allowed performance figure into subsystem or component level contributions. Note that the addition of contributions is not always linear; systematic effects add linear, stochastic effect add quadratic.

These budgets are based on models of the system. Of course every model is a simplification of reality. Figure 7 shows the many components in the system that in one way or the other influence the overlay. It is immediately clear that the overlay budget takes only a limited set of influences into account, the "significant" ones.

When the performance requirements of the system increase (as dictated by

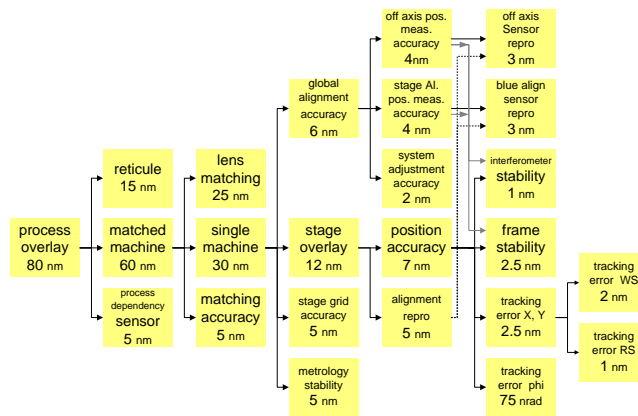


Figure 6: Overlay budget (1999)

Moore's law) more and more components start to fall into the *significant* category, causing an exponential increase of adjustment and control complexity.

### Overlay Influence Diagram.

(Maarten Bonnema, 19-3-1999)

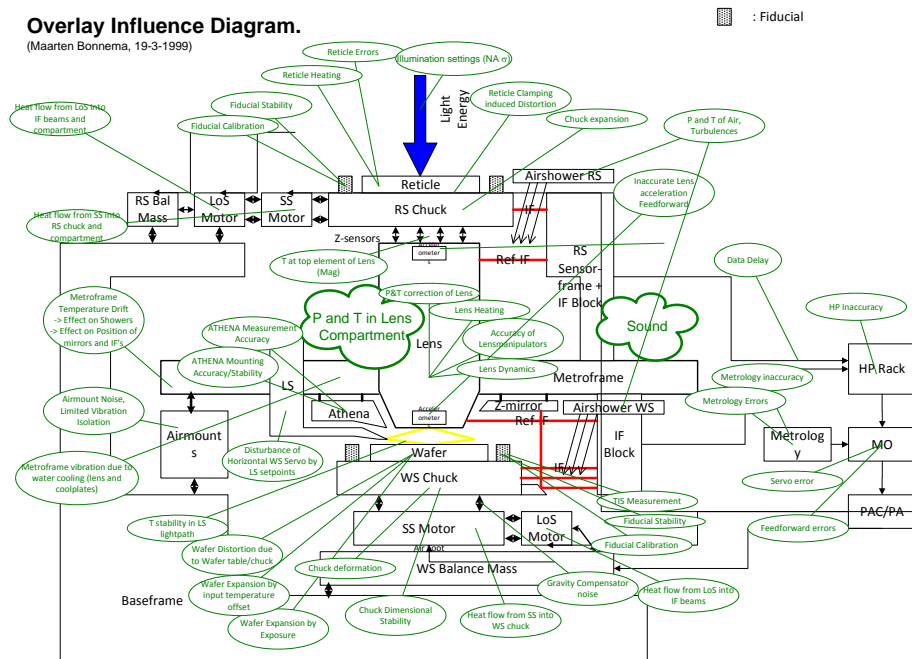


Figure 7: Everything influences overlay

## 2 Problem statement

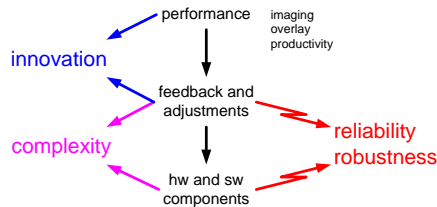


Figure 8: Challenge: Exponential Increase

The exponential increase of the performance requirements inherently cause an exponential increase of the system complexity. This in itself is a tremendous managerial challenge. However the increase of complexity threatens to decrease the reliability dramatically, while the reliability is not allowed to decrease from customer point of view.

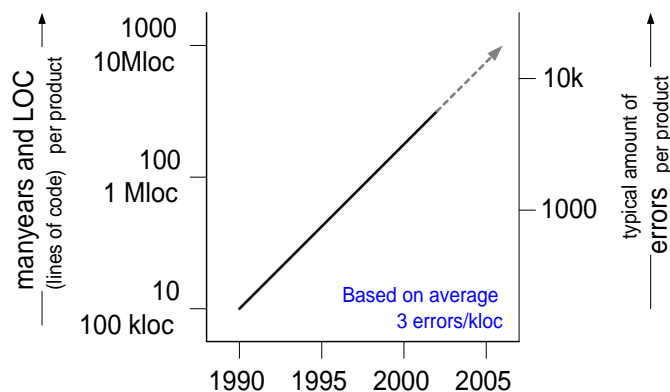


Figure 9: The Software Reliability Threat

For the software contribution to system failures the relation between complexity and reliability is visualized in figure 9. In zero order approximation the software grows exponential, and since the fault density in practice stays constant, the number of errors in the code also grows exponential. Most of these faults never show up at all, however, sometimes the changing use cause an epidemic appearance of the same fault accross many machines at the same time.

clearpage

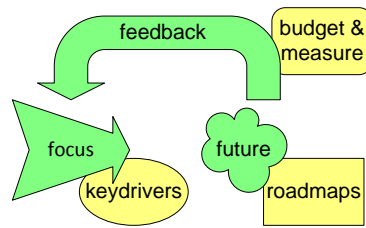


Figure 10: Success factor: ASML system engineering style

### 3 ASML style system engineering

ASML tackles the challenging problem of exponential performance increase and maintaining a reliable system by applying system engineering in an ASML specific way. Figure 10 shows the main ingredients of this style:

- Feedback[4]
- Focus[1]
- Future awareness[2]

#### 3.1 Feedback

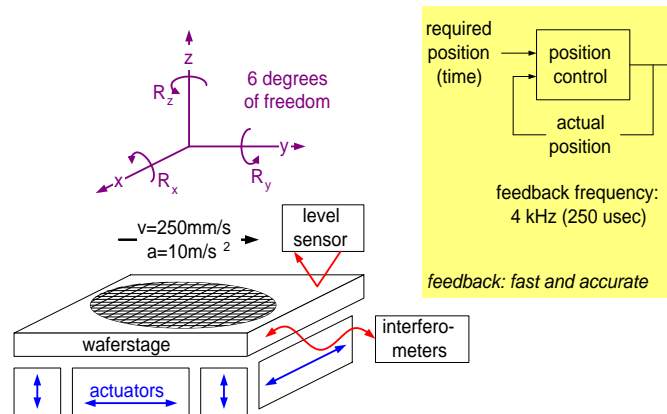


Figure 11: Feedback as technical design pattern

Feedback is a well known engineering pattern. Figure 11 shows an example of the use of feedback in the waferstepper itself. The high positioning accuracy can only be obtained by more or less continuous feedback. The current generation of wafersteppers uses feedback to control 6 degrees of freedom for the wafer stage.



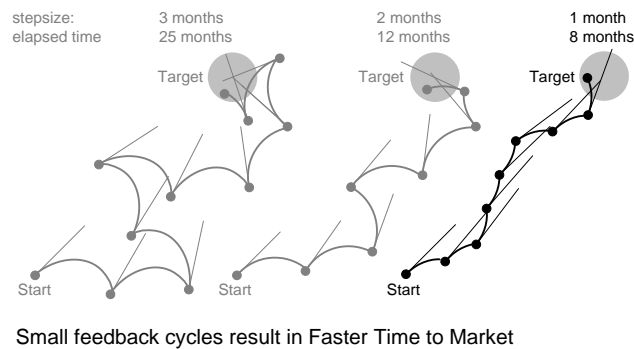


Figure 12: Feedback as development process pattern

Feedback as part of the development process is also crucial. Figure 12 shows the effect of the feedback cycle time on the total elapsed time of a project. If a project is late in obtaining feedback it is likely to be derailed significantly. The figure clearly visualizes that small increments are much more efficient than large leaps without feedback.

ASML is applying this development feedback at many levels, for instance via early integration. An important part of the product strategy is also feedback oriented: early availability of new technologies for the customers, which provides customer feedback to ASML, while it enables the customer to explore the new technologies.

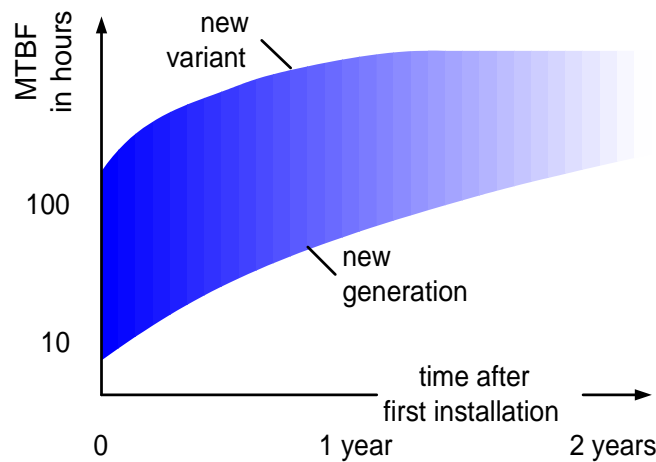


Figure 13: MTBF as function of time

The uptime is one of the important aspects to fulfill the productivity. The uptime of new generation systems in general is quite low for the first time shipments.

However the early shipment is important for both ASML as well as the customer, as explained above. The uptime is quickly improving after the first shipment, due to the learning effect, see figure 13

### 3.2 Focus

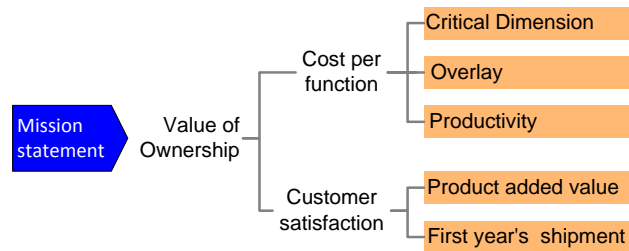


Figure 14: Focus via key drivers

Clear communication about the customer and the company objectives provides focus for the development team. The focus is articulated by means of customer key drivers, which are translated into requirements and technology decisions. Part of this derivation is shown in figure 14.

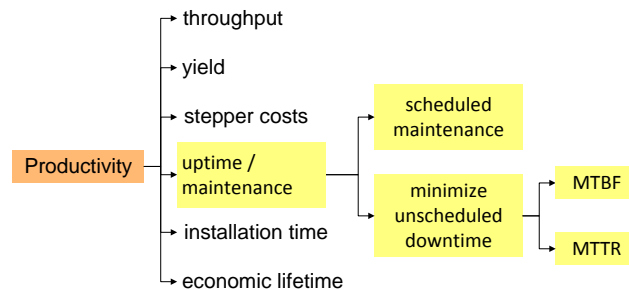


Figure 15: Productivity decomposed

Figure 15 shows the next level of decomposition of the productivity key driver. Many reliability aspects become visible here. From productivity point of view unscheduled downtime is undesirable, this often severely disturbs the manufacturing flow. Scheduled downtime for preventive maintenance or replacement of consumables is not too bad.

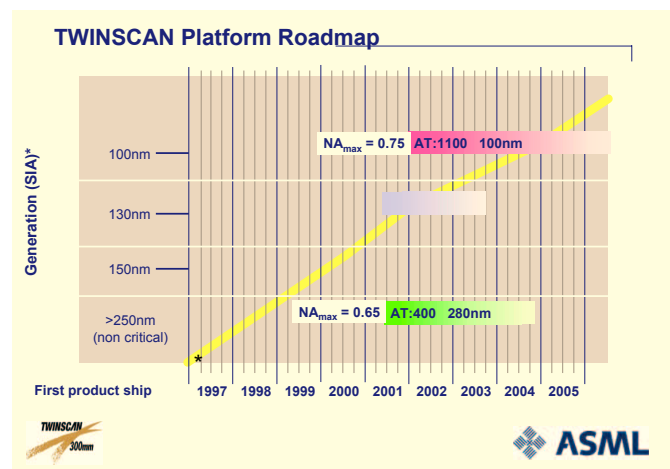


Figure 16: Future aware

### 3.3 Future awareness

Many of the technological challenges which are facing lithography suppliers require new technologies and sometimes inventions. The lead time for the required technology development is so long that the balance between short term needs (products out) and long term needs (availability of the right technologies) is critical. Vision of the future is required to start timely with new technologies. ASML uses roadmaps to articulate the vision on the future, figure 16 shows one of these roadmaps.

## 4 Conclusion

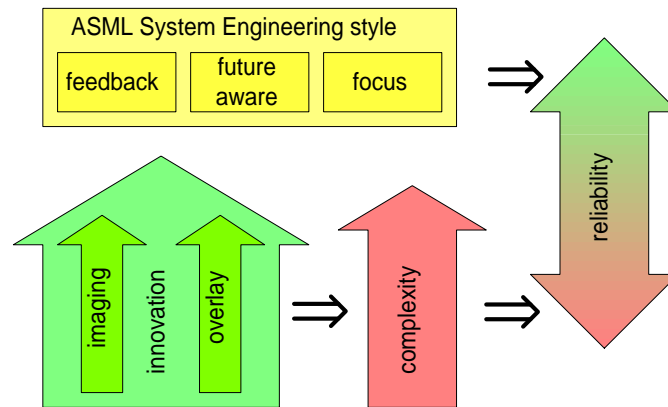


Figure 17: Conclusion

Figure 17 shows the conclusion: The ever increasing innovation, for wafer-steppers the ever increasing imaging and overlay, result in increase of complexity. This complexity increase threatens the reliability. ASML counters this threat by applying a system engineering approach, with emphasis on feedback, focus and future awareness.

## 5 Acknowledgements

William van der Sterren pointed out a number of inconsistencies and unclarities.

## References

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## **History**

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- Added case disclaimer
- changed status to finished